

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

| | | |
|-------------------------|---|-------------------------------|
| LG DISPLAY CO., LTD., |) | |
| |) | |
| Plaintiff, |) | Civil Action No. 06-726 (JJF) |
| |) | Civil Action No. 07-357 (JJF) |
| v. |) | |
| |) | CONSOLIDATED CASES |
| CHI MEI OPTOELECTRONICS |) | |
| CORPORATION, et al. |) | |
| |) | |
| Defendants. |) | |
| |) | |

**APPENDIX OF EXHIBITS TO CHI MEI OPTOELECTRONICS'
ANSWERING MEMORANDUM REGARDING
PROPOSED CLAIM CONSTRUCTIONS**

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IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

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EXHIBIT C-9



US005327001A

United States Patent [19][11] **Patent Number:** **5,327,001****Wakai et al.**[45] **Date of Patent:** **Jul. 5, 1994**

[54] **THIN FILM TRANSISTOR ARRAY HAVING SINGLE LIGHT SHIELD LAYER OVER TRANSISTORS AND GATE AND DRAIN LINES**

[75] **Inventors:** Haruo Wakai, Fussa; Nobuyuki Yamamura, Hachioji; Syunichi Sato, Kawagoe; Minoru Kanbara, Hachioji, all of Japan

[73] **Assignee:** Casio Computer Co., Ltd., Tokyo, Japan

[21] **Appl. No.:** 41,537

[22] **Filed:** Apr. 1, 1993

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Related U.S. Application Data

[63] Continuation of Ser. No. 734,017, Jul. 22, 1991, abandoned, which is a continuation of Ser. No. 503,455, Apr. 2, 1990, abandoned, which is a continuation-in-part of Ser. No. 241,304, Sep. 7, 1988, Pat. No. 5,032,883.

[51] **Int. Cl.⁵** H01L 27/01; H01L 27/13; H01L 29/78

[52] **U.S. Cl.** 257/350; 257/354; 359/59; 359/88

[58] **Field of Search** 357/23.7, 30 L; 359/59, 359/87, 88; 257/347, 350, 352, 353, 354

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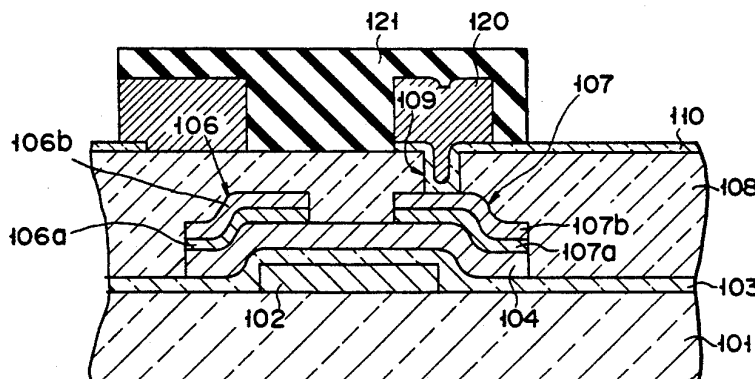
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Primary Examiner—Ngan Ngo
Attorney, Agent, or Firm—Frishauf, Holtz, Goodman & Woodward

[57]

ABSTRACT

A TFT array has a plurality of gate lines and a plurality of drain lines formed on a transparent insulating substrate. The gate lines intersect with the drain lines. TFTs are formed at the intersections of the gate lines and the drain lines. An opaque film is formed above the gate lines, the drain lines, and the TFTs, allowing no passage of light passing through the gaps between the transparent electrode, on the one hand, and the gate and drain lines, on the other hand. Therefore, when the TFT array is incorporated into a liquid-crystal display, the display will display high-contrast images.

8 Claims, 14 Drawing Sheets

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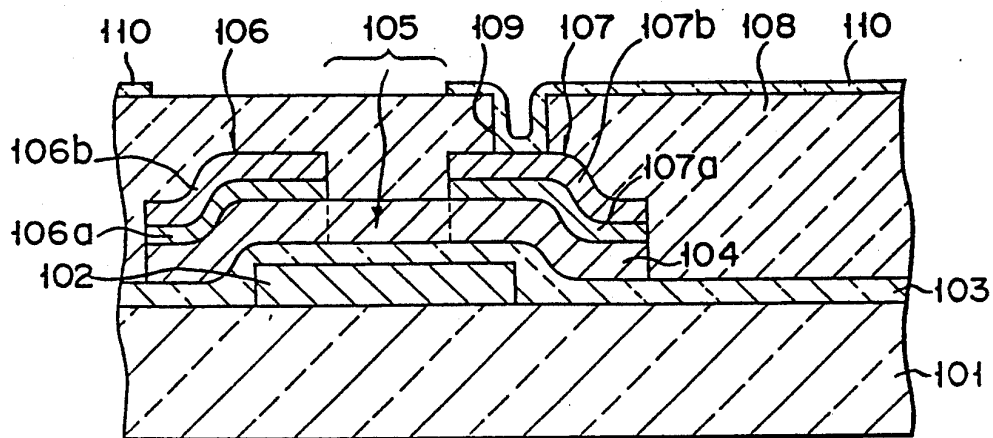


FIG. 3

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FIG. 4A

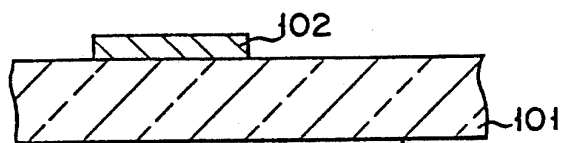


FIG. 4B

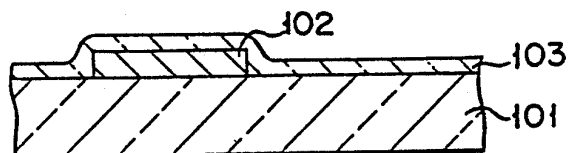


FIG. 4C

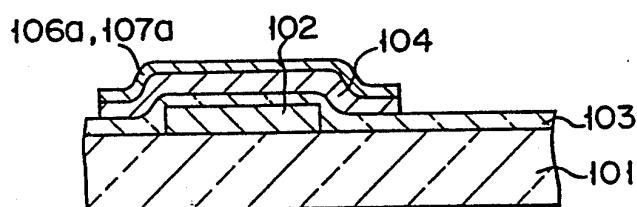


FIG. 4D

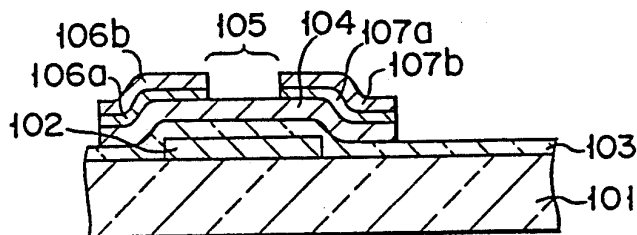


FIG. 4E

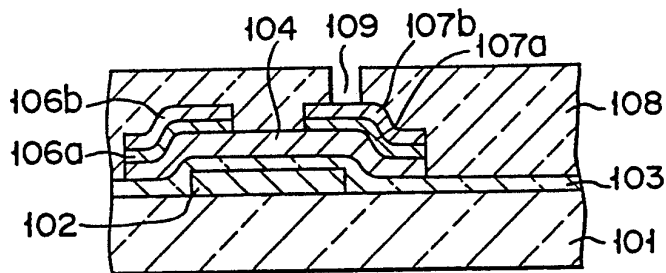
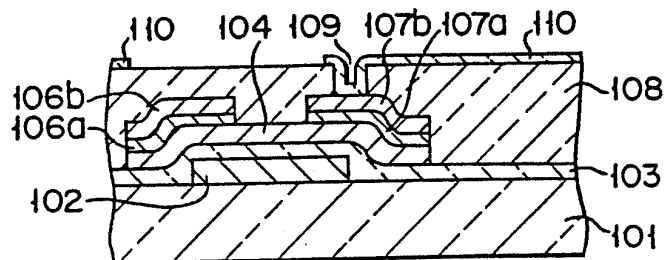


FIG. 4F



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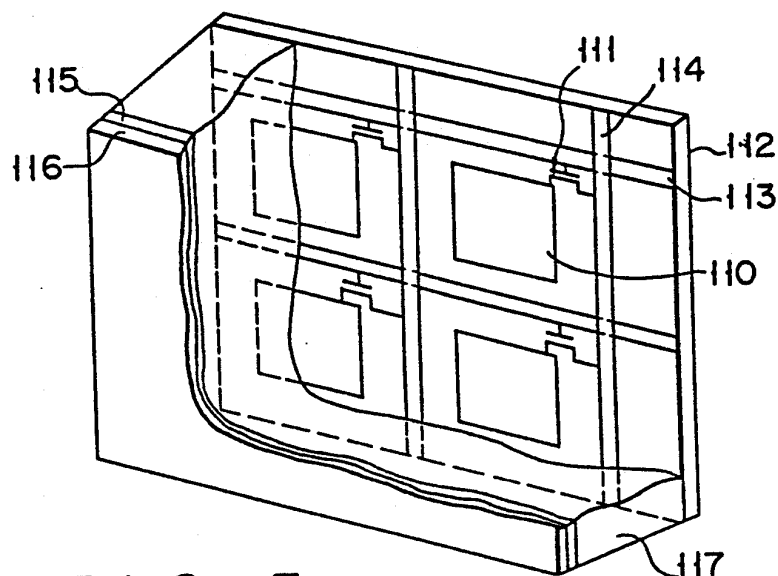


FIG. 5

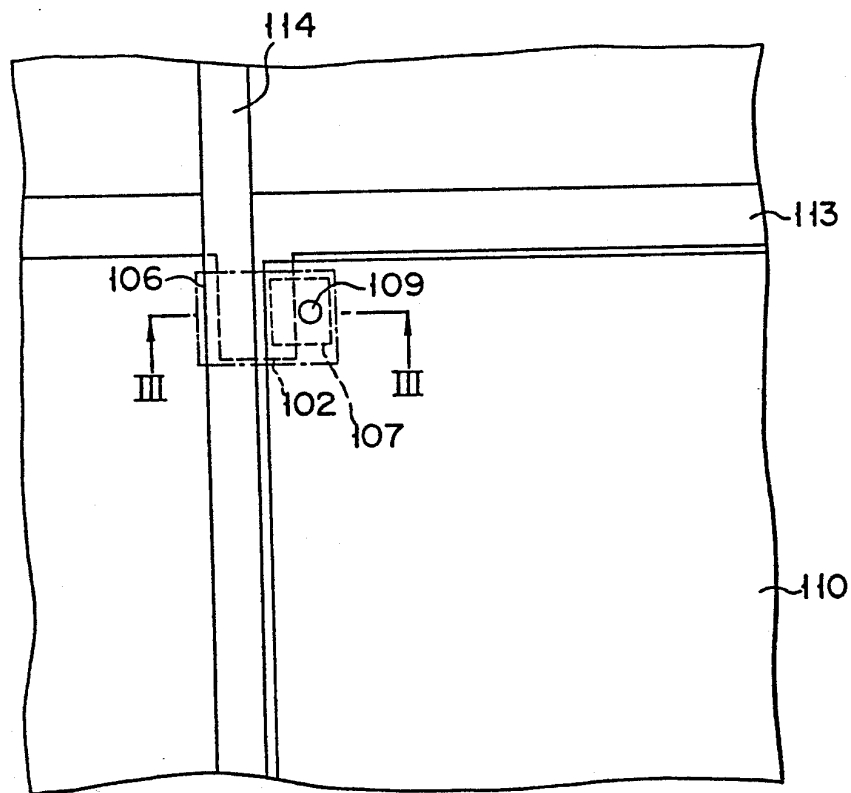


FIG. 6

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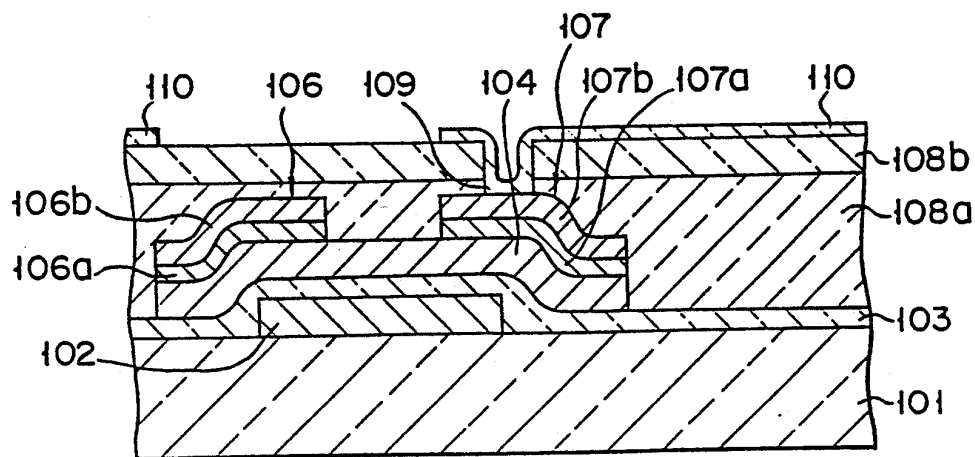


FIG. 7

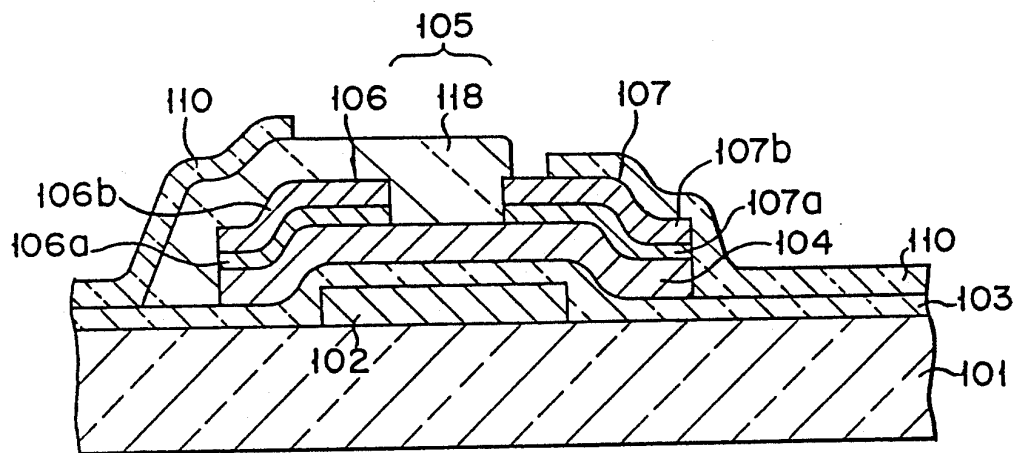


FIG. 8

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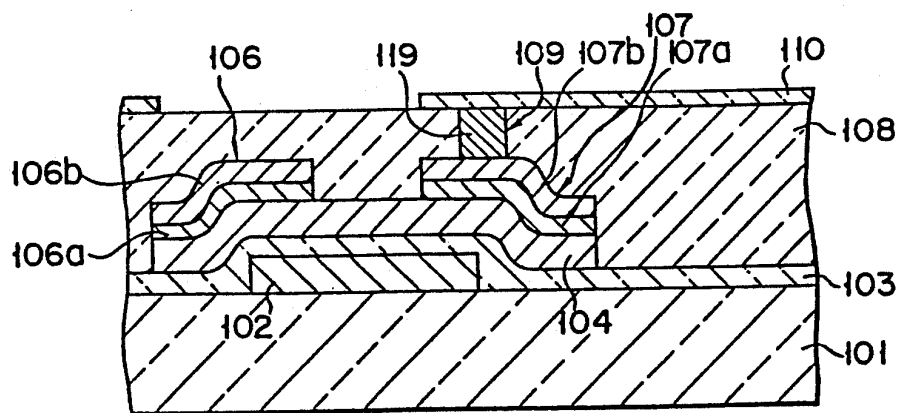


FIG. 9

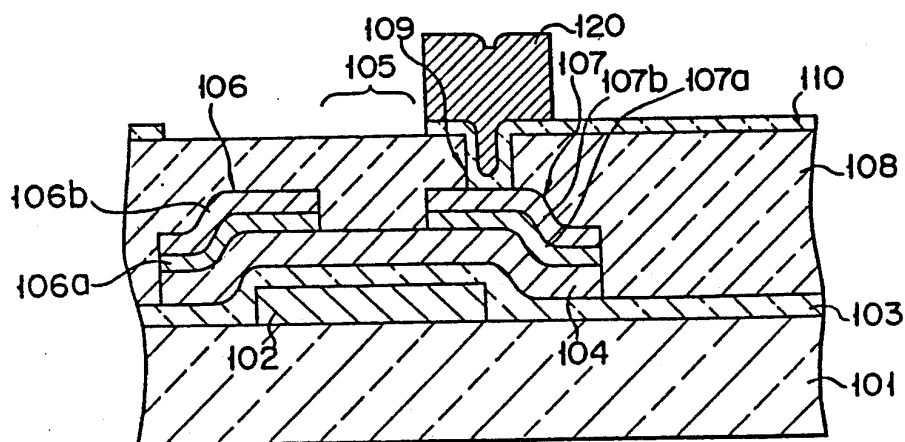


FIG. 10

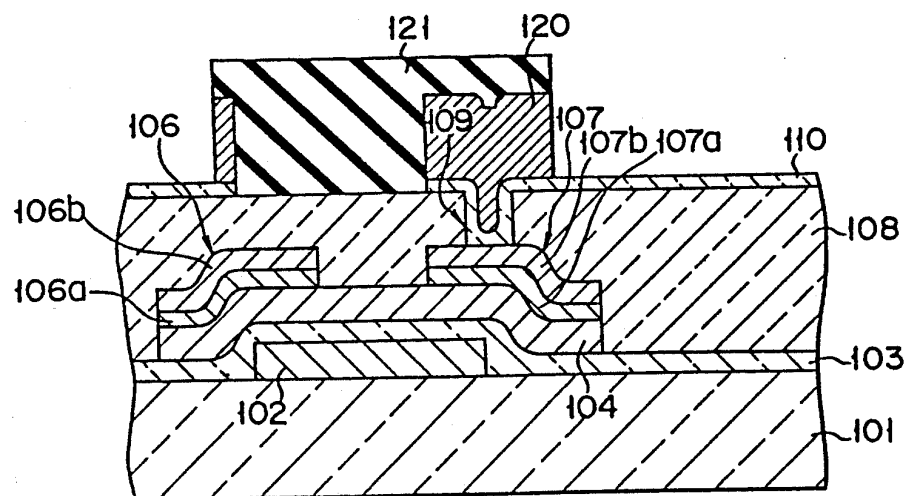


FIG. 11

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FIG. 12A

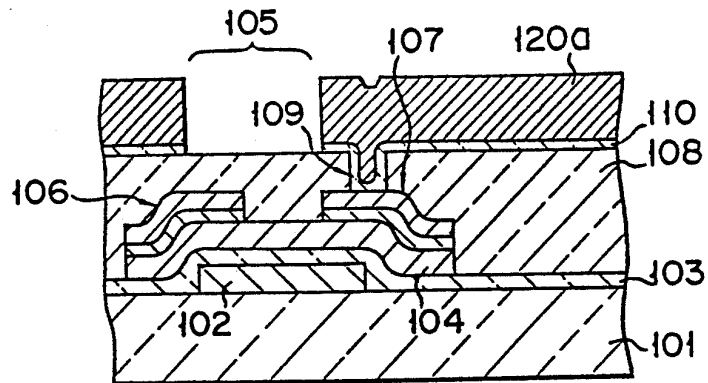


FIG. 12B

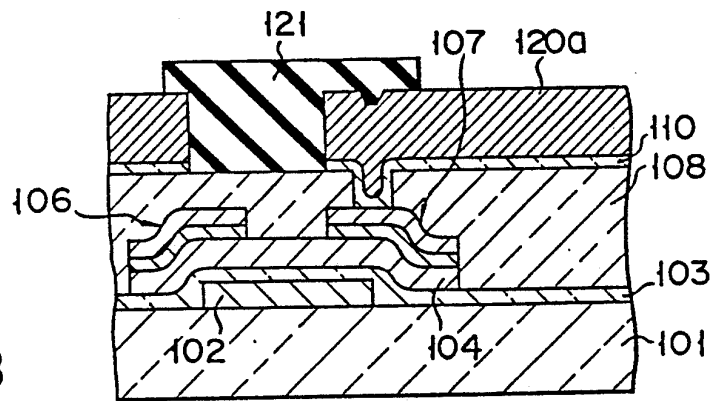
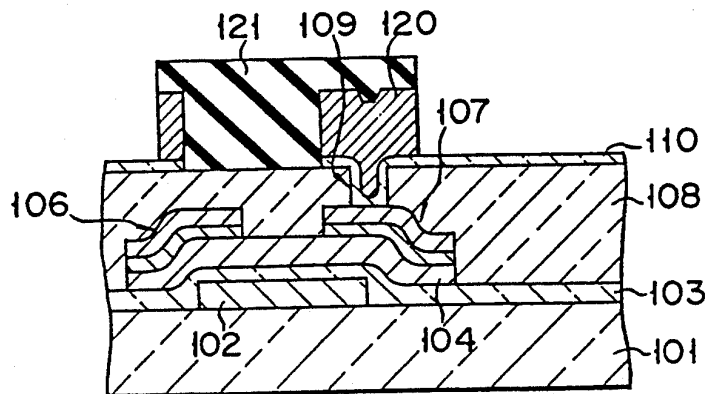


FIG. 12C



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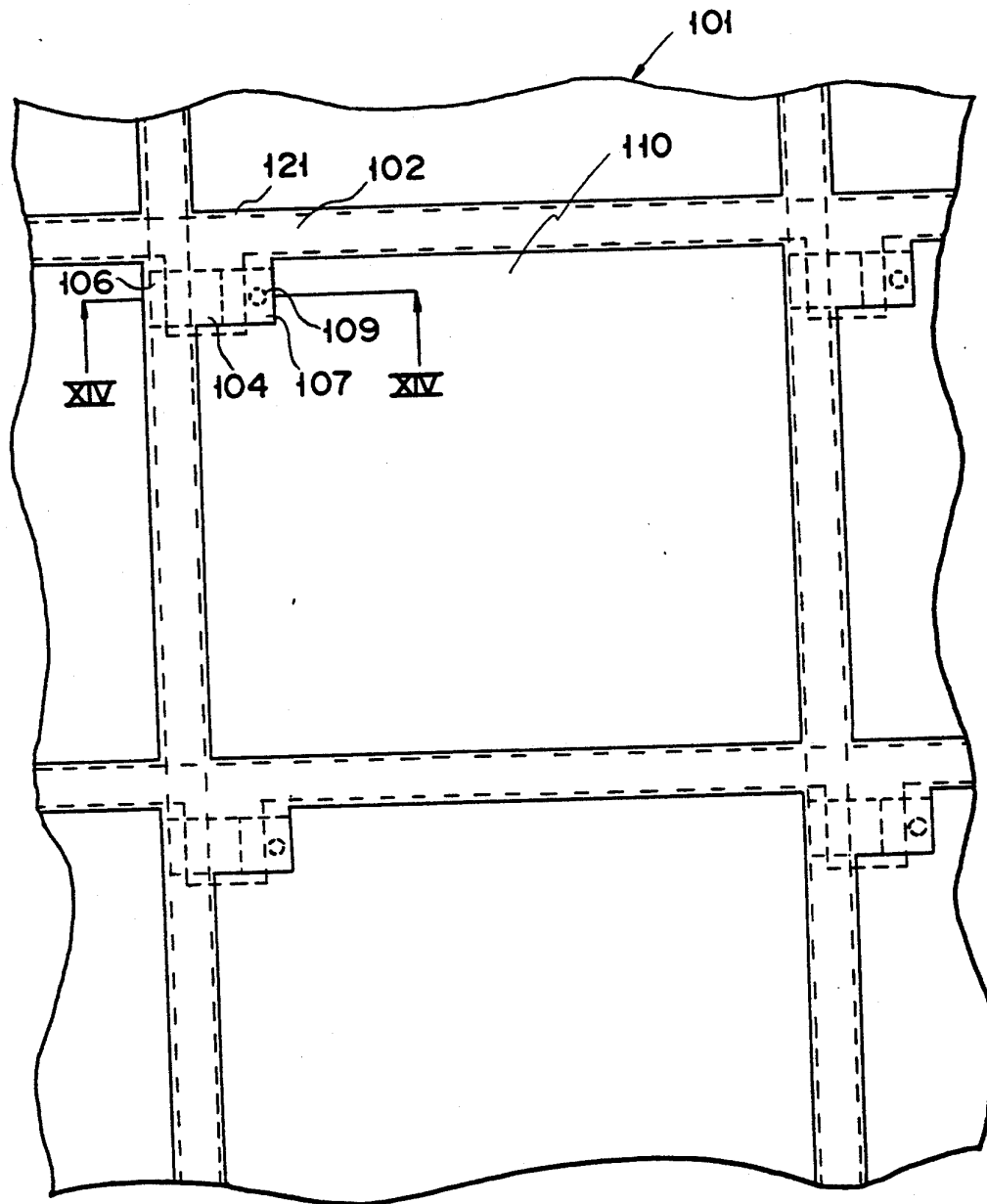


FIG. 13

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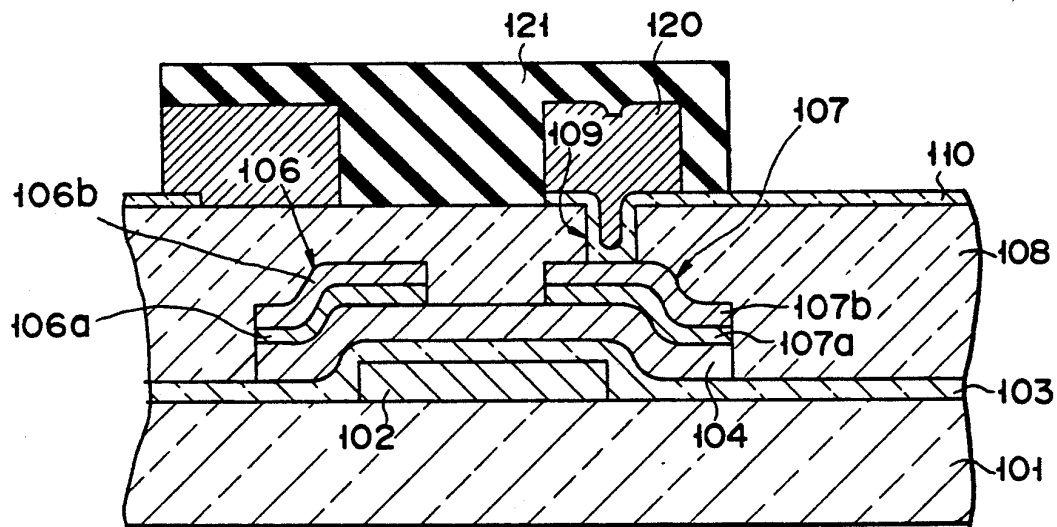


FIG. 14

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FIG. 15A

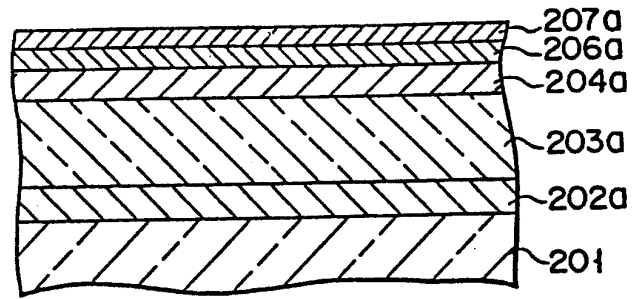


FIG. 15B

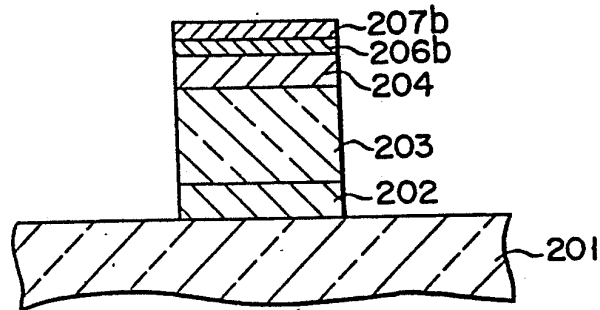


FIG. 15C

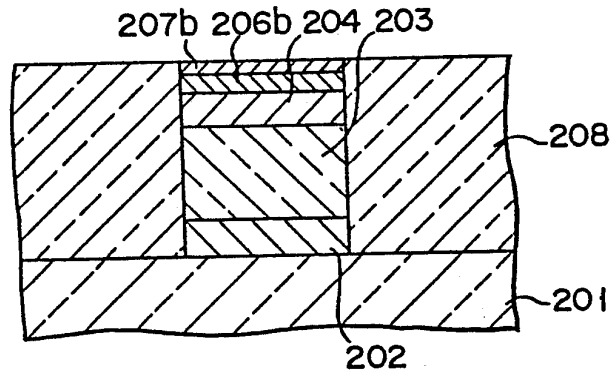
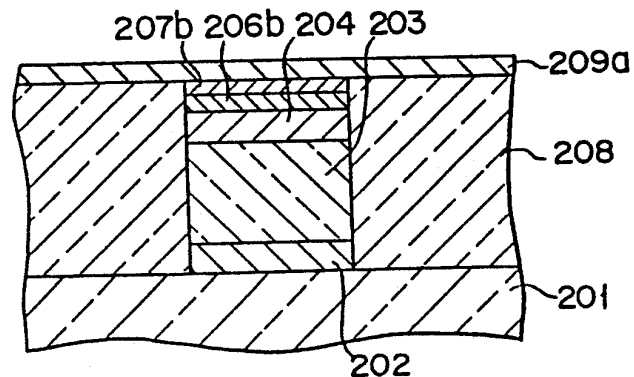


FIG. 15D



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FIG. 15E

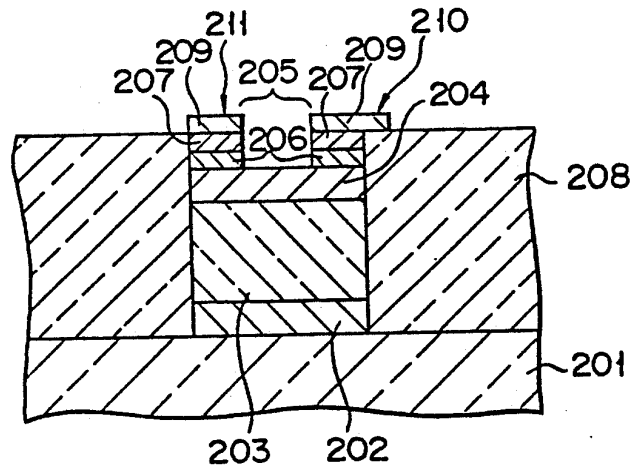


FIG. 15F

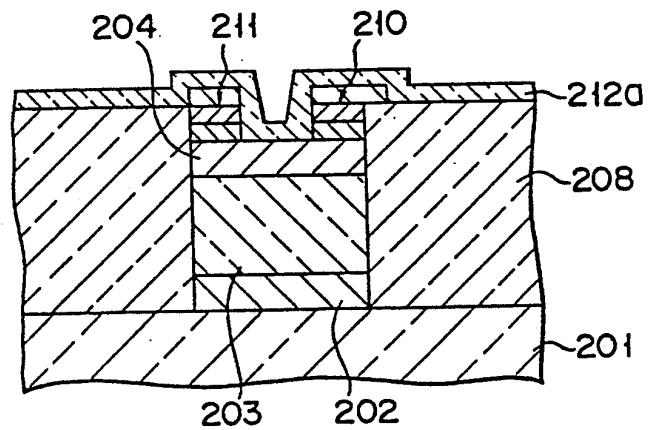
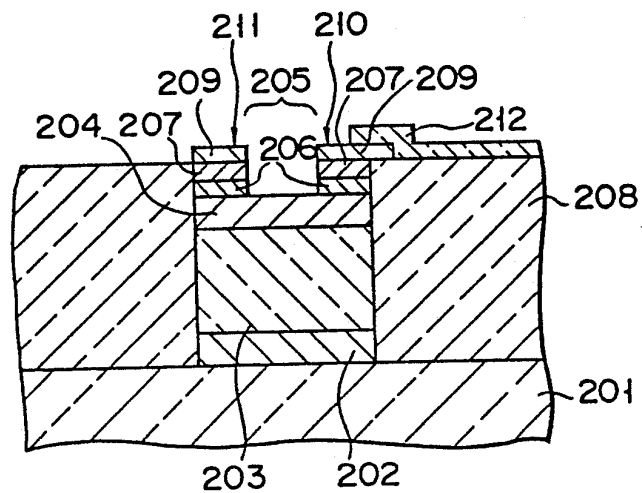


FIG. 15G



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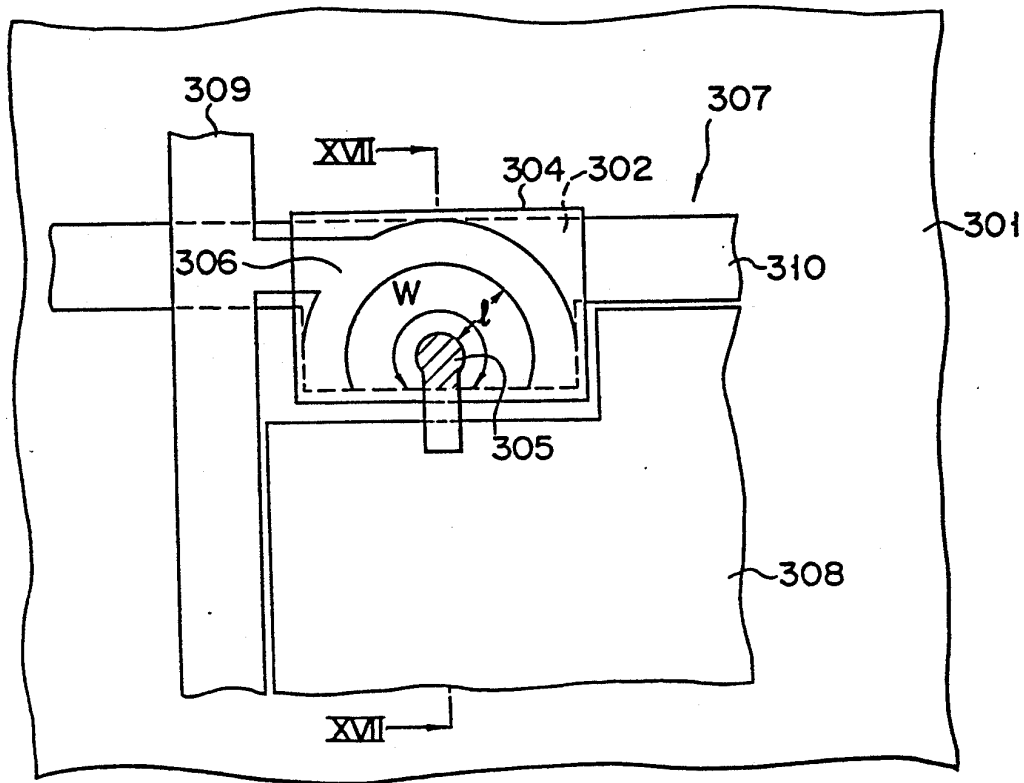


FIG. 16

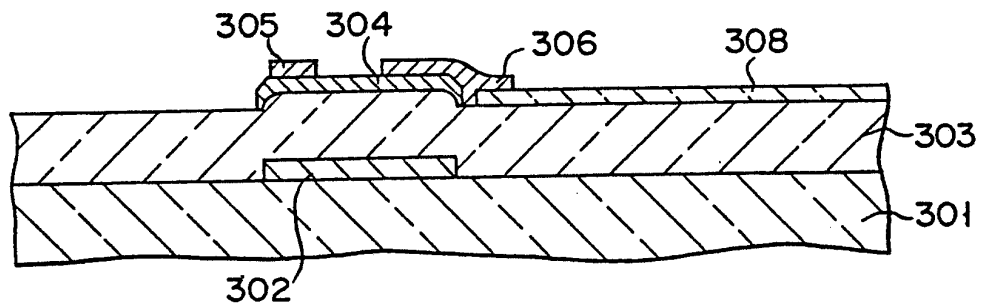


FIG. 17

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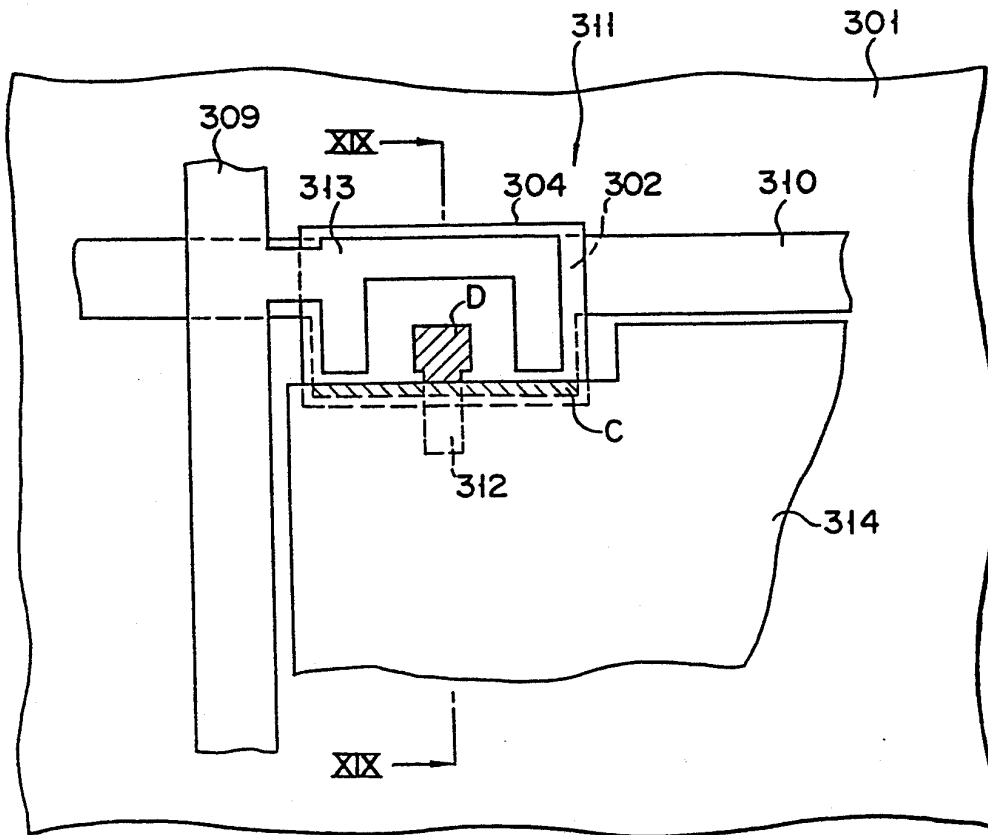


FIG. 18

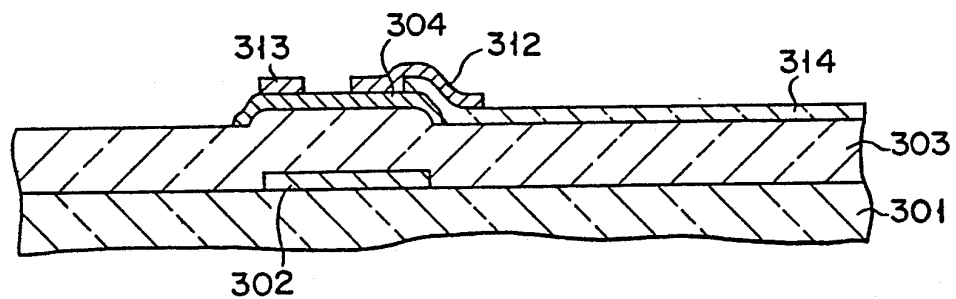


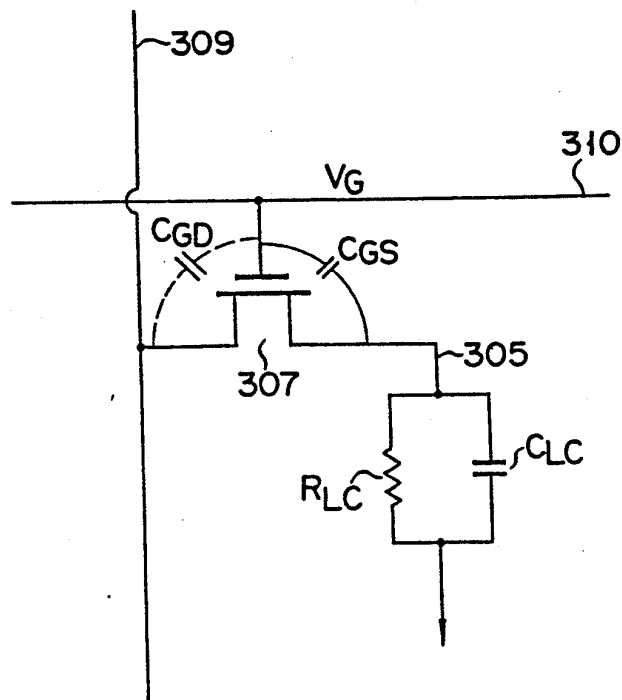
FIG. 19

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THIN FILM TRANSISTOR ARRAY HAVING SINGLE LIGHT SHIELD LAYER OVER TRANSISTORS AND GATE AND DRAIN LINES

CROSS-REFERENCES TO THE RELATED APPLICATIONS

This application is a continuation, of application Ser. No. 07/734,017, filed Jul. 22, 1991, (abandoned) which is a Continuation of Ser. No. 07/241,304, filed Sep. 7, 1988 (now U.S. Pat. No. 5,032,883 issued Jul. 16, 1991).

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a TFT (Thin Film Transistor) array having a plurality of TFTs arranged in the form of a matrix, and each having a pixel electrode and made by stacking a gate electrode, a semiconductor layer, a source electrode, a drain electrode, and the like, on a transparent insulation substrate.

2. Description of the Related Art

Conventional TFTs as switching elements are disclosed in published Examined Japanese Utility Model Application No. 44-5572 (U.S. Ser. No. 132095), Published Examined Japanese Patent Application No. 41-8172 (U.S. Ser. No. 344921), and P.K. Weimer, "The TFT - A New Thin-Film Transistor", PROCEEDINGS OF THE IRE, Jun. 15 1962. Liquid crystal display panels using such TFTs are disclosed in "A 6×6 Inch 20 lines-Per-Inch Liquid Crystal Display Panel", IEEE Transactions on Electron Device, vol. ED-20, No. Nov. 11, 1973 and U.S. Pat. No. 3,840,695.

On the other hand, U.S. Pat. Nos. 3,765,747 and 3,862,360, and Published Unexamined Japanese Patent Application Nos. 55-32026, 57-20778, and 58-21784 disclose a technique wherein a MOS transistor is formed on a monocrystalline semiconductor substrate, and the resultant structure is used as one of the substrates of a liquid crystal display panel. However, if liquid crystal panels are constituted by these semiconductor substrates, only reflection type displays can be obtained. In addition, the manufacturing processes of such panels are as complex as that of LSIs. Moreover, it is difficult to obtain a large display panel.

The above-described active matrix liquid crystal panels, therefore, have the TFTs used as switching elements. The structures of these TFTs can be classified into a coplanar type, an inverted coplanar type, a staggered type, and an inverted staggered type, as disclosed in the article by P.K. Weimer. Of these types, the inverted staggered type TFT can be formed by stacking a plurality of thin films successively in a vacuum. For this reason, the number of manufacturing steps is substantially decreased. As a result, the characteristics of a product are stabilized, and the rate of occurrence of defective transistors is decreased.

FIGS. 1 and 2 show structures of the above-described inverted staggered type TFT and a TFT array obtained by arranging a plurality of such inverted staggered type TFTs on an insulating substrate. Referring to FIGS. 1 and 2, a plurality of TFTs 1 are arranged on a transparent insulating substrate 2 in the form of a matrix. Gate electrodes 3 of TFTs 1 are connected by a gate line 4 extending in the row direction. Drain electrodes 5 of TFTs 1 are connected by a drain line 6 extending in the column direction. A source electrode 7 of each TFT 1 is connected to a transparent electrode 8 independently formed in an area surrounded by the gate and drain lines

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4 and 6 (an electrode, to which a data signal is supplied, will be referred to as a drain electrode hereinafter). More specifically, as shown in FIG. 2, the gate electrode 3 consisting of Cr or the like is formed on the transparent glass substrate 2, and a gate insulating film 9 consisting of silicon oxide or silicon nitride is formed on the upper surface of the glass substrate 2 including the upper surface of the gate electrode 3. A semiconductor film 10 consisting of amorphous silicon is stacked on the gate insulating film 9 above the gate electrode 3. Drain and source electrodes 5 and 7 are formed on the semiconductor film 10. They are separated from each other by a predetermined distance, forming channel portion 11. Drain and source electrodes 5 and 7 respectively have contact layers 5a and 7a, and metal layers 5b and 7b, and are electrically connected to the semiconductor 10. The source electrode 7 is connected to the transparent electrode 8 consisting of Indium-Tin-Oxide (to be referred to as an ITO hereinafter).

In the TFT used for the above-described TFT array, since part of the drain electrode 5, the drain line 6, and the transparent electrode 8 are formed on the gate insulating film 9, both the electrodes tend to be short-circuited, and hence the rate of occurrence of defects becomes high. Especially in the TFT array using this TFT, since the transparent electrode 8 is formed in a region surrounded by the gate and drain lines 4 and 6, short-circuiting tends to occur between the transparent electrode 8 and the drain line 6.

In order to prevent such short-circuiting, the transparent electrode 8 and the drain line 6 are spaced apart for a distance L determined by process and alignment precision in forming the transparent electrode 8 and the drain line 6. The distance L is as long as 20 μm or more.

No transparent electrodes extend over the distance L. Hence, when the TFT array is incorporated into a liquid crystal display, no voltage is applied to that portion of the liquid-crystal layer which extends over this distance L. Light therefore passes through this portion of the liquid-crystal layer, whereby the display inevitably has a low contrast.

To prevent light from passing through said portion of the liquid-crystal layer, a black mask is formed on the entire back of the substrate of the TFT array, except for that portion on which the transparent electrode is formed. (The transparent electrode is made of a transparent metal or a transparent resin.) Because of the presence of the black mask, the liquid-crystal display can have a sufficient contrast. However, the forming of the black mask requires a manual operation, and the black mask is usually displaced with respect to the transparent electrode. Consequently, light passes through a part of the transparent electrode, reducing not only the image contrast, but also the brightness of the display screen. For example, when the black mask is displaced by 20 μm with respect to the transparent electrode the opening ratio of the pixels will decrease to 50%.

SUMMARY OF THE INVENTION

The present invention has been made to solve the problem described above, and its object is to provide a TFT array which serves to provide a liquid-crystal display having high contrast, though it has black masks.

In order to achieve this object, a TFT array according to the invention comprises:

a transparent substrate;

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a plurality of gate lines formed on the transparent insulating substrate;

a plurality of drain lines formed on the transparent insulating substrate and intersecting with the gate lines; thin film transistors located at the intersections of the gate lines and the drain lines, each having at least a gate electrode, a semiconductor layer having a channel portion, a source electrode, and a drain electrode;

a transparent electrode electrically connected to the source electrodes of the thin film transistors; and an opaque film overlapping the gate lines and the drain lines.

Due to the opaque film formed on the gate lines and the drain lines, all formed on the transparent electrode, there is no gap between the transparent electrode, on the one hand, and the gate lines and drain lines, on the other, for allowing the passage of light. Hence, the TFT array serves to provide a liquid crystal display which has high contrast. Further, since the opaque film is formed also on the channel portions of the TFTs, the TFTs are not influenced by light, making no errors at all. Since the opaque film is formed on the entire surface of the substrate, it can be patterned in a single process, and the TFT array can, thus, be manufactured easily.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view showing a conventional TFT; FIG. 2 is a sectional view illustrating the TFT, taken along line II—II in FIG. 1;

FIG. 3 is a sectional view showing an inverted staggered TFT having a pixel electrode formed on the upper surface;

FIGS. 4A to 4F are sectional views explaining the steps of manufacturing the TFT shown in FIG. 3;

FIG. 5 is a partly broken-away perspective view showing a liquid crystal display element comprising the TFT shown in FIG. 3;

FIG. 6 is a partially enlarged view illustrating an array of a plurality of TFTs;

FIG. 7 is a sectional view representing a first modification of the TFT shown in FIG. 3;

FIG. 8 is a sectional view showing a second modification of the TFT shown in FIG. 3;

FIG. 9 is a sectional view showing a third modification of the TFT shown in FIG. 3;

FIG. 10 is a sectional view showing a fourth modification of the TFT shown in FIG. 3;

FIG. 11 is a sectional view showing a fifth modification of the TFT shown in FIG. 3;

FIGS. 12A to 12C are sectional views explaining how the TFT shown in FIG. 11 is manufactured;

FIG. 13 is a plan view of a TFT array according to the present invention;

FIG. 14 is a sectional view showing the TFT array shown in FIG. 13, taken along line XIV—XIV in FIG. 13;

FIGS. 15A to 15G are sectional views explaining the steps of manufacturing a TFT array according to the present invention;

FIG. 16 is a plan view showing the structure of another type of a TFT for use in the present invention;

FIG. 17 is a sectional view showing the TFT shown in FIG. 16, taken along line XVII—XVII in FIG. 16;

FIG. 18 is a plan view illustrating another type of a TFT for use in the present invention;

FIG. 19 is a sectional view showing the TFT illustrated in FIG. 18, taken along line XIX—XIX in FIG. 18; and

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FIG. 20 is an equivalent circuit diagram of a liquid crystal display element comprising the TFTs shown in FIGS. 16 and 18.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A TFT for use in the invention, which is an inverted staggered TFT having a pixel electrode, will now be described with reference to the accompanying drawings.

FIG. 3 is a sectional view illustrating the inverted staggered TFT. A gate electrode 102 consisting of Cr and having a thickness of about 1,000 Å is formed on an insulating substrate 101 consisting of a transparent glass plate. A gate insulating film 103 made of silicon nitride or silicon oxide and having a thickness of about 3,000 Å is formed on the upper surface of the insulating substrate 101 including the upper surface of the gate electrode 102. A semiconductor film 104 consisting of amorphous silicon and having a thickness of about 1,000 Å is formed on the gate insulating film 103, covering a portion above the gate electrode 102 and its peripheral portion. Drain and source electrodes 106 and 107 are formed on the semiconductor film 104. They are separated from each other by a predetermined distance, thus forming a channel portion 105. In order to electrically connect the drain and the source electrodes 106 and 107 to the semiconductor film 104, the electrodes 106 and 107 are respectively constituted by the contact films 106a and 107a, each made of amorphous silicon doped with an impurity in a high concentration and having a thickness of about 500 Å, and conductive layers 106b and 107b, each made of a conductive metal material such as Cr and having a thickness of about 1,000 Å. In addition, a transparent insulating film 108 made of SiO₂, polyimide, or an acrylic resin is deposited on substantially the entire exposed surface above the insulating substrate 101 on which the above-described films are stacked in a predetermined form. The drain electrode 106 is covered with the insulating film 108 and is insulated from other electrodes. The thickness of the insulating film 108 on the drain and the source electrodes 106 and 107 is about 3,000 Å. The insulating film 108 fills recesses generated upon formation of the above thin films, thereby smoothening the surface above the insulating substrate 101. A through hole 109 extending through the insulating film 108 is formed in a portion of the insulating film 108 above the source electrode 107. In addition, a transparent electrode 110 consisting of ITO and having a thickness of about 1,000 Å is formed on the upper surface of the insulating film 108. The transparent electrode 110 extends into the through hole 109 and hence is electrically connected to the source electrode 107. A portion of the transparent electrode 110 above a channel portion 105 of the semiconductor film 104 formed between the drain and the source electrodes 106 and 107, and its portion above the drain electrode 106 is mostly removed. That is, the transparent electrode 110 above the channel portion 105 must be removed so as to prevent an unnecessary electric field from being applied to the channel portion 105. Furthermore, in order to decrease a parasitic capacitance, the transparent electrode 110 is formed above the drain electrode 106, with its edge slightly overlapping the edge of the drain electrode 106. Note that since the parasitic capacitance is small, the transparent electrode 110 may overlap the drain electrode 106. If the thickness of the insulating film 108 formed on the drain and

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the source electrodes 106 and 107 is excessively small, the insulation property is degraded. In contrast to this, if it is excessively large, connection to the transparent electrode through hole 109 formed on the source electrode 107 will be difficult. For this reason, the thickness of the insulating film 108 preferably falls within the range of 2,000 to 8,000 Å.

In the TFT having the above structure, since the insulating film 108 is formed at least on the drain electrode 106, the probability of short-circuiting between the drain and the source electrodes 106 and 110 is considerably decreased. In addition, since the transparent electrode 110 is not present above the channel portion 105 of the semiconductor film 104, an unnecessary electric field is not applied to the channel portion 105, and hence the TFT can be stably operated.

With reference to FIGS. 4A to 4F it will now be explained how the TFT shown in FIG. 3 is manufactured.

As shown in FIG. 4A, a metal film having a thickness of, e.g., about 1,000 Å is deposited by means of sputtering or vapor deposition on the transparent insulating substrate 101 having a cleaned surface. The metal film is patterned by photolithography or the like to form the gate electrode 102. The insulating substrate 101 may consist of glass, quartz, sapphire, or the like. The gate electrode 102 consists of chromium, titanium, tungsten, tantalum, copper, or the like.

As shown in FIG. 4B, the gate insulating film 103 is then formed on the entire surface of the insulating substrate 101 by plasma CVD or the like so as to have a thickness of, e.g., 3,000 Å and cover the gate electrode 102. A silicon nitride (SiN) film, silicon oxide (SiO₂) film, or the like is used as the gate insulating film 103. Subsequently, as shown in FIG. 4C, the semiconductor film 104 made of amorphous silicon (a-i-Si) or the like and the contact film 106a (107a) made of amorphous silicon (a-n⁺-Si) which is doped with an impurity at high concentration are continuously formed/stacked by plasma CVD or the like on the gate insulating film 103 so as to have thicknesses of, e.g., 1,000 Å and 500 Å, respectively. The semiconductor film 104 and the contact film 106a (107a) are patterned by photolithography or the like so as to cover a portion above the gate electrode 102 and its peripheral portion. Instead of the above amorphous silicon, amorphous silicon carbide (SiC), tellurium, selenium, germanium, cadmium sulfide (CdS), cadmium selenide (CdSe), or the like may be used as a material for semiconductor film 104 and contact film 106a (107a).

A 1,000-Å thick metal film is then formed on the entire surface above the insulating substrate 101 by vapor deposition, sputtering, or the like, thus covering the contact film 106a (107a). The metal film is patterned by photolithography or the like to remove the contact film 106a (107a) above the channel portion 05, thereby forming the drain and the source electrodes 06 and 107 above the gate electrode 102, which are separated from each other by a predetermined distance, as shown in FIG. 4D. Chromium, titanium, tungsten, tantalum, copper, or the like is used as a material for the metal films 106b and 107b of the drain and the source electrodes 106 and 107.

As shown in FIG. 4E, the transparent insulating film 108 is formed above the insulating substrate 101, covering at least the drain electrode 106 and smoothening the surface. As the transparent insulating film 108, an organic insulating film obtained by coating and baking

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polyimide or an acrylic resin using a spin coat method, or an SiO₂ inorganic insulating film (SOG film) obtained by spin-coating and baking a silanol compound. The thickness of the transparent insulating film 108 on the drain electrode 106 is about 3,000 Å. Subsequently, the through hole 109 is formed in the transparent insulating film 108 above the source electrode 107 by etching.

Finally, as shown in FIG. 4F, a transparent conductive material such as ITO, tin oxide (SnO₂), or indium oxide (In₂O₃) is sputtered on the surface of the transparent insulating film 108 including the through hole 109 to a thickness of about 1,000 Å. Then, portions of this transparent conductive material above the channel portion 105 of the semiconductor film 104 and overlapping the drain electrode 106 through the transparent insulating film 108 are removed. With the above process, fabrication of the TFT is completed.

According to the above-described manufacturing method, since the step of forming the transparent electrode 110 in which a defect generally tends to occur becomes the last step, even if a defect occurs in this step, the immediately preceding step can be repeated, thereby reducing the ratio of occurrence of defects.

As shown in FIGS. 5 and 6, a plurality of TFTs of FIG. 3 are arranged on a transparent insulating substrate in the form of a matrix, and are used as a liquid crystal display device. More specifically, a plurality of TFTs 111 are arrayed on a transparent insulating substrate 112 in the column and the row directions. Gate electrodes 102 of the respective TFTs are commonly connected to gate line 113 in the row direction. Drain electrodes 106 of the respective TFTs are commonly connected to drain line 114 in the column direction. Source electrodes 107 of TFTs 111 are connected to transparent electrodes 110, which are substantially formed into squares, through through holes 109. Transparent electrodes 110 are respectively arranged in a plurality of regions surrounded by the gate and the drain lines 113 and 114, and are electrically independent from each other. The edges of each transparent electrode 110 are located near the gate and the drain lines 113 and 114, or slightly overlap them. The above-described sectional structure shown in FIG. 3 corresponds to a sectional structure taken along line III—III in FIG. 6.

An opposite transparent substrate 116 having a transparent electrode 115 formed on its entire surface is placed on the substrate on which TFTs 111 are arranged in the form of a matrix in the above-described manner so as to oppose it. A liquid crystal display device is obtained by sealing liquid crystal 117 between these substrates. In this liquid crystal display device, one transparent electrode 110 is a pixel electrode corresponding to one pixel for image display. These pixel electrodes do not overlap the channel portions of the TFTs connected to the adjacent pixel electrodes, and areas where the pixel electrodes overlap the corresponding drain electrodes are minimized.

The above-described liquid crystal display device is operated in the following manner. Scan signals are sequentially supplied to a plurality of the gate lines 113. Data signals for controlling the ON/OFF states of the respective pixels are supplied to a plurality of the drain lines 114 in accordance with the timings of the scan signals. TFT 111 whose gate electrode 102 has received a scan signal is turned on, reads a data signal supplied at that timing, and supplies it to the pixel electrode 110.

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An electric field is applied to the liquid crystal 117 located between the pixel electrode which has received the data signal and the transparent electrode 115 of the opposite substrate 116 in accordance with a potential difference between the opposite electrodes. Then, the orientation state of the molecules of the liquid crystal 117 is changed, and thus transmission and interception of light are controlled.

As described above, in the liquid crystal display having pixel electrodes on TFTs, the transparent insulating film 108 is formed on at least the drain electrode 106 of the TFT, and the transparent electrode 110 is formed on the resultant structure. Therefore, short circuiting between the transparent electrode 110 and the drain electrode 106 can be prevented. In addition, the distance between the transparent electrode 110 and the drain electrode 106, i.e., distance L in FIG. 1, can be set to be zero. Moreover, the transparent electrode 110 may be arranged so as to overlap the drain and the gate lines 114 and 113. With this arrangement, the entire region except for an opaque region (the semiconductor film 104, the source and the drain electrodes 107 and 106, and the gate and the drain lines 113 and 114) can be made an effective display area, and hence a maximum effective display area can be obtained. According to the embodiment, an opening ratio of 70% can be realized (50% in the conventional device). Since the step of forming the transparent electrode is the last one, and the source electrodes of all the TFTs are commonly connected upon deposition of the transparent conductive film before the step of separating the transparent conductive film individually is executed operations of all the TFTs can be measured within a short period of time by bringing the probe of a measuring device into contact with a plurality of the gate and the drain lines 113 and 114, and the transparent conductive film and supplying test signals.

Modifications of the TFT shown in FIG. 3 will be described with reference to FIGS. 7 and 8. The same reference numerals in these drawings denote the same parts as FIG. 3, and a description thereof will be omitted.

FIG. 7 illustrates the first modification of the TFT shown in FIG. 3. A first and a second insulating films 108a and 108b are deposited to cover a drain and a source electrodes 106 and 107, and a transparent electrode 110 is formed on the resultant structure. The first insulating film 108a is an SiO₂ film obtained by dissolving a silanol compound in a solvent, coating the resultant solution by a spin coat method, and baking the coated film. The first insulating film 108a is used to flatten the uneven surface above an insulating substrate. The second insulating film 108b is a nitride film obtained by chemical vapor deposition (CVD), and is used to improve an insulation property. In the first modification of the TFT, the surface above an insulating substrate 101 can be reliably smoothened, and the insulation property and the like can be reliably protected.

FIG. 8 illustrates the second modification of the TFT shown in FIG. 3. A transparent electrode 110 is formed without flattening the surface above an insulating substrate 101. An insulating film 118 is formed on only a channel portion 105 and a drain electrode 106 so as to protect the channel portion 105 and insulate the drain electrode 106 from the transparent electrode 110. Accordingly, the transparent electrodes 110 of one TFT and an adjacent TFT are not present above the channel portion 105, and the area where the transparent elec-

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trode 110 overlaps the drain electrode 106 is small. Therefore, short-circuiting between the transparent electrode 110 and the drain electrode 106 does not occur, and an electric field is not applied from the transparent electrode 110 to the channel portion 105.

FIG. 9 shows the third modification of the TFT shown in FIG. 3. A contact metal 119 consisting of a conductive metal material is buried in a through hole 109 formed above a source electrode 107, and a transparent electrode 110 is deposited on the resultant structure, thereby electrically connecting the source electrode 107 to the transparent electrode 110. The contact metal 119 consists of nickel, gold, silver, chromium, or the like, and is formed in the through hole 109 by electroless plating. In the third modification, the source and the transparent electrodes 107 and 110 are connected to each other through the contact metal 119. Therefore, electrical connection therebetween can be ensured.

FIG. 10 illustrates the fourth modification of the TFT shown in FIG. 3. A contact metal 120 consisting of chromium, copper, aluminum, or the like is stacked on a transparent electrode 110, which is electrically connected to a source electrode 107, formed in a through hole 109 of a transparent film 108. In the fourth modification, electrical connection between the source and the transparent electrodes 107 and 110 can be ensured.

FIG. 11 shows the fifth modification of the TFT shown in FIG. 3. A shield film 121 is formed above a contact metal 120, a channel portion 105, and a drain electrode 106 shown in the fourth modification so as to prevent a decrease in OFF resistance of the TFT due to radiation of external light onto the channel portion 105.

The contact metal 120 and a shield film 121 in the fifth modification are formed in the following manner. As shown in FIG. 12A, a transparent electrode film made of ITO and having a thickness of 500 to 1,000 Å and a metal conductive film 120a consisting of chromium, copper, or aluminum and having a thickness twice the depth of a through hole 109, e.g., about 6,000 Å are continuously stacked on the surface above an insulating substrate 101 including a transparent insulating film 108 and the through hole 109, and parts of the stacked films above the channel portion 105 and on a drain electrode 106 are removed. Subsequently, as shown in FIG. 12B, a shield material consisting of a nontransparent and insulating resin or a metal oxide is stacked on the resultant structure. Then, the shield material is etched so as to be left on regions including a region above the through hole 109 of the metal conductive film 120a and a region above the channel portion 105, thereby forming a shield film 121. After this process, as shown in FIG. 12C, the metal conductive film 120a is etched by using the shield film 121 as a resist to remove the metal conductive film 120a from the surface of the transparent electrode 110, thereby forming the contact metal 120 on the through hole 109.

In the conventional TFT array shown in FIG. 1, which is used in a liquid-crystal display, the gate line and the drain line 6 are spaced apart from the transparent electrode 8 by a distance L. Light passes through the gap between the lines 4 and 5, on the one hand, and the transparent electrode 8. Consequently, the liquid-crystal display has but an insufficient contrast.

FIGS. 13 and 14 are a plan view and a sectional view of a TFT array according to the invention, wherein good use is made of a shield film of the type shown in FIG. 11, thereby eliminating the gap between the gate and drain lines, on the one hand, and the transparent

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electrode, thereby to impart a sufficient contrast to the liquid-crystal display.

As is illustrated in FIG. 13, a plurality of gate lines 102 is formed on a transparent insulating substrate 101. A plurality of drain lines 106 is also formed on the substrate 101, intersecting with the gate lines 102. TFTs are located at the intersections of the gate lines 102 and the drain lines 106.

As is evident from FIG. 14, each of the TFTs comprises a gate electrode 102 (i.e., a part of the gate line 101), a semiconductor layer 104, a source electrode 107, and a drain electrode 106 (i.e., a part of the drain line 106). A transparent electrode 110 is formed on a transparent insulating film 108 and extends through a contact hole cut in the film 108, thus being electrically connected to the source electrode 107. A shield film 121, which is an opaque film, is formed partly on the exposed surface of the insulating film 108 and partly on the transparent electrode 110. The shield film 121 is located above the gate line 102, the drain line 106, and the channel portion of the semiconductor film 104. It should be noted that the shield film 121 is not spaced from the transparent electrode 110.

As can be understood from FIG. 13, the shield film 121 extends over the gap between the transparent electrode 110, on the one hand, and the gate and drain lines 102 and 106, on the other. Hence, no light passes through the gap between the electrode 110 and the lines 102 and 106. The liquid-crystal display having this TFT array can therefore have high contrast.

As is best shown in FIG. 14, which is sectional view taken along line XV—XV in FIG. 13, the gate lines 102 are formed on the substrate 101, and the gate insulating film 103 is formed also on the substrate 101 and the gate lines 102. Further, the semiconductor layer 104 is formed on the gate insulating film 103, opposing the gate electrode 102. The source electrode 106 and the drain electrode 107 are formed on the ends of the semiconductor layer 104, respectively.

The transparent insulating film 108 covers the thin transistors (TFTs), and has a smooth upper surface. The contact hole 107 is made in the film 108. A contact 120 made of metal is formed on the transparent electrode 110 and is partly filled in the contact hole 107. The shield film 121 is formed, covering the exposed surface of the film 108, a part of the electrode 110, and the contact 120.

Since the shield film 121 is located above the channel portion of the semiconductor layer 104, it protects the TFT from light, thus preventing the TFT from making errors.

As has been described, the shield film 121 is located above the gate lines 102, the drain line 106, and the TFTs (i.e., the channels portions of the layer 104). It allows no passage of light passing through the gap between the electrode 110, on the one hand, and the gate and drain lines 102 and 106. Therefore, when the TFT array shown in FIGS. 13 and 14 is incorporated into a liquid-crystal display, the display can display high-contrast images. Moreover, since the shield film 121 is formed easily, first by forming an opaque film on the entire surface of the substrate 101 and then patterning the opaque film.

FIGS. 15A to 15G show the steps of manufacturing this TFT. FIG. 15G shows a finished TFT. As shown in FIG. 15G, in the TFT, a gate electrode 202, a gate insulating film 203, and a semiconductor film 204 are stacked on a transparent insulating substrate 201 and

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formed into the same shape. A contact films 206 each consisting of a semiconductor layer having a high impurity concentration, an ohmic contact electrodes 207, and a metal electrodes 209, all pairs of which have the identical shapes, are formed on the semiconductor film 204 and separated from each other by a predetermined distance to form a channel portion 205. A drain and a source electrodes 211 and 210 are respectively constituted by the contact films 206, the ohmic contact electrodes 207, and metal electrodes 209. A transparent insulating film 208 is formed on a portion outside the stacked thin films to the height of the ohmic contact electrode 207. In addition, a pixel electrode 212 is formed on the transparent insulating film 208 so as to be in contact with the metal electrode 209 of the source electrode 210.

The TFT having the above-described arrangement is manufactured in the following manner. As shown in FIG. 15A a metal film 202a consisting of chromium (Cr) molybdenum (Mo), tungsten (W), or the like is deposited on a cleaned surface of the transparent insulating substrate 201 to a thickness of, e.g., 1,000 Å by sputtering, vapor deposition, or the like. An insulating film 203a made of silicon nitride (SiN) or the like is deposited on the metal film 202a to a thickness of, e.g., about 3000 Å by plasma CVD or the like. Subsequently, an amorphous silicon (a-i-Si) film 204a and a n⁺-type amorphous silicon (a-n⁺-Si) film 206a doped with a high-concentration impurity are respectively deposited on the resultant structure to thicknesses of, e.g., about 1,000 Å and 500 Å by plasma CVD or the like. In addition, an ohmic contact film 207a consisting of Cr, Ti, a noble metal silicide such as PTSi or PT₂Si, or the like for an ohmic contact is deposited on the n⁺-type amorphous silicon 206a by sputtering or the like. The steps of stacking/forming the metal film 202a, the insulating film 203a, the amorphous silicon 204a, the n⁺-type amorphous silicon 206a, and the ohmic contact film 207a on the transparent insulating substrate 201 are continuously performed by sputtering and plasma CVD.

As shown in FIG. 15B, the ohmic contact film 207a, the n⁺-type amorphous silicon 206a, the amorphous silicon 204a, the insulating film 203a, and the metal film 202a are etched to form the gate electrode 202, a gate line (not shown) for supplying scan signals to the gate electrode 202, the gate insulating film 203, the semiconductor film 204, the contact film portion 206b, and the ohmic contact electrode film 207b. The ohmic contact film 207a the n⁺-type amorphous silicon 206a the amorphous silicon 204a, the insulating film 203a, and the metal film 202a are continuously etched by, e.g., reactive etching. Alternatively, the n⁺-type amorphous silicon 206a, the amorphous silicon 204a, the insulating film 203a may be etched by plasma etching, the and metal film 202a may be etched by wet etching. Then, as shown in FIG. 15C, the transparent insulating flattening film 208 consisting of a silica film or an organic substance such as acrylic is coated above the transparent insulating substrate 201 to a height substantially equal to that of the ohmic contact electrode film 207b by a spin coating method.

If the flattening film 208 is also coated on the ohmic contact electrode film 207b upon coating the flattening film 208 on the film 207b is removed by etch back.

In addition, a metal film 209a having a small specific resistance, such as an aluminum (Al), copper (Cu), or silver (Ag) film, is deposited on the entire surfaces of

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the ohmic contact electrode film 207b and the flattening film 208 above the transparent insulating substrate 201 by sputtering, vapor deposition, or the like. Then, as shown in FIG. 13E, the corresponding position of the channel portion 205 of the metal film 209a, the ohmic contact metal film 207b, and the contact film portion 206b is continuously etched respectively by photolithography to form the drain and the source electrodes 211 and 210 each consisting of the metal electrode 209, the ohmic contact electrode 207, and the contact film 206, and to form a drain line for supplying image signals to the drain electrode 211.

Subsequently, as shown in FIG. 15F, a transparent conductive film 212a such as an ITO film is deposited on the entire surface above the transparent insulating substrate 201 by vapor deposition or the like.

Finally, as shown in FIG. 15G, a pixel electrode 212 is formed by photolithography or the like. With this process, a TFT active matrix panel is completed. In the TFT of this embodiment, since the gate electrode 202, the gate insulating film 203, the semiconductor film 204, the contact film 206, and the ohmic contact electrode 207 can be successively formed in a series of steps, stable characteristics can be obtained. Since the stacked films obtained by the above-described series of steps are continuously etched, the number of steps is decreased.

A structure of another TFT will be described below. FIGS. 16 and 17 show this TFT. More specifically, a gate electrode 302 is formed on a glass substrate 301, 10 and a gate insulating film 303 consisting of silicon nitride and having a thickness of about 3,000 Å is stacked on the gate electrode 302. A semiconductor film 304 consisting of amorphous silicon is stacked on part of the gate insulating film 303, which corresponds to the gate electrode 302. A circular source electrode 305 is formed on the semiconductor film 304. The source electrode 305 has a diameter of, e.g., about 4 μm. A drain electrode 306 is formed in an annular shape on the semiconductor film 304 substantially concentrically with the source electrode 305, thereby forming a semiconductor channel portion in a partial annular shape between the two electrodes. Since the channel portion is formed so as to surround the source electrode 305, if the distance between the two electrodes is a channel length L, and the length of an arc defined by substantially intermediate points of the channel length L is a channel width W, the channel width W is sufficiently larger than the channel length L. Ratio L/W of channel length L to channel width W is one or less.

A plurality of TFTs 307 each arranged in the above-described manner are arrayed on the substrate 301 in the form of a matrix. The source electrode 305 of TFT 307 is connected to a pixel electrode 308 consisting of a transparent conductive substance. The drain electrodes 306 of TFTs 307 arranged in the column direction are commonly connected to a drain line 309. The gate electrodes 302 of TFTs 307 arranged in the row direction are commonly connected to a gate line 310. In addition, a plurality of pixel electrodes 308 connected to source electrodes of TFTs 307 are arrayed above the glass substrate 301 in the form of a matrix.

In TFT 307, the source electrode 305 is formed so as to be smaller than the drain electrode 306. Therefore, the area where the source and the gate electrodes 305 and 302 overlap each other is considerably smaller than that where the drain and the gate electrodes 306 and 302 overlap each other. As indicated by an equivalent circuit diagram in FIG. 20, gate-source capacitance CGS

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present between the gate and the source electrodes 302 and 305 is very small. If, for example, the source electrode 305 is a circular electrode having a diameter 4 μm and the gate insulating film 303 has a thickness of 3,000 Å as is the case with this embodiment, a gate-source capacitance CGS is as small as about 0.003 PF. Assuming that an equivalent capacitance CLC between two electrodes opposing each other through the pixel electrode 308 and a corresponding liquid crystal is set to be 0.1 PF (in a case wherein the area of the pixel electrode 308 is 100 μm × 100 μm), then a voltage drop ΔV across the source electrode 305 can be represented by:

$$\Delta V = \{C_{GS} / (C_{GS} + C_{LC})\} \cdot V_g = \{0.003 / (0.003 + 0.1)\} \cdot V_g$$

This voltage drop is as small as about 3% of gate voltage Vg. As described above, since the area of the source electrode 305 is made small in this TFT, the gate-source capacitance CGS can be made small compared with the capacitance generated between one pixel electrode and an electrode opposing the pixel electrode through a liquid crystal. Therefore, the influences of gate signals on source potentials can be reduced, and the pixel electrode 308 can be micropatterned. In addition, since the drain electrode 306 is formed so as to surround the source electrode 305, the channel width can be increased, and high drive performance of a thin film transistor can be realized.

A structure of a TFT according to still another embodiment will be described with reference to FIGS. 18 and 19. Since the fundamental structure of this TFT is the same as that of the TFT in FIGS. 16 and 17, the same reference numerals in FIGS. 18 and 19 denote the same parts as in FIGS. 16 and 17, and a description thereof will be omitted. Referring to FIGS. 18 and 19, a source electrode 312 of TFT 311 has a rectangular shape. U-shaped a drain electrode 313 is formed so as to surround rectangular the source electrode 312. Similarly, in TFT 311, the area of the source electrode 312 is made small, and hence the area where the source and the gate electrodes 312 and 302 overlap each other is small. Therefore, a gate-source capacitance CGS between the gate and the source electrodes 302 and 312 is small, and the influence of a gate signal on a source potential is small. In addition, since a drain electrode 313 is formed so as to surround the source electrode 312, a channel width can be set to be sufficiently large.

Furthermore, in order to increase the opening ratio by increasing the area of a pixel electrode 314 as much as possible, the pixel electrode 314 is extended so that it partially overlaps the gate electrode 302 as indicated by cross-hatched portions in FIG. 18. In this case, the gate-source capacitance CGS between the gate and the source electrodes 302 and 312 is determined by the sum of areas D and C where the gate and the source electrodes 302 and 312, and the gate and the pixel electrodes 312 and 314 overlap each other, as indicated by the cross-hatched portions in FIG. 18. Therefore, area C where the gate and the pixel electrodes 302 and 314 overlap each other, and area D where the gate and the source electrodes 302 and 312 overlap each other are determined such that gate-source capacitance CGS determined by areas C and D becomes sufficiently small compared with an equivalent capacitance CLC between one pixel electrode 314 and an electrode opposing the pixel electrode 314 through a liquid crystal.

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Note that the source and the drain electrodes 312 and 313 may be formed into polygonal shapes without an acute angle, such as a pentagon and a hexagon, or elliptical shapes.

What is claimed is:

1. A thin film transistor array, comprising:

a single substrate;

a plurality of thin film transistors formed on said single substrate, each thin film transistor having at least a gate electrode, a semiconductor layer having a channel portion and a source electrode and a drain electrode;

a plurality of gate lines and a plurality of drain lines provided over said single substrate in an intersecting relation via an insulating film, said gate lines and drain lines being connected to gate and drain electrodes of the transistors at locations near the respective intersections of the gate and drain lines;

a plurality of transparent electrodes electrically connected to the source electrodes and providing a matrix array arranged in a plurality of regions surrounded with the gate and drain lines, respectively;

a transparent insulating film formed at least on said thin film transistor, said gate lines and said drain lines, said transparent insulating film having a first surface which is in contact at least with said thin film transistors and said gate and drain lines, and a second surface which is an opposite surface opposing said first surface; and

a single light shield film formed on said second surface of said transparent insulating film, said single light shield film being over said single substrate so as to cover the channel portions of said transistors, said gate lines, and said drain lines, and said single light shield film having a width which is not less than an interval between adjacent peripheral edges of said plurality of transparent electrodes, so as to overlap the edges of said plurality of transparent electrodes, to thereby shield said channel portions from light and to shut off light leaking from among a plurality of transparent electrodes.

2. A thin film transistor array according to claim 1, wherein said light shield film is formed of a resin.

3. A thin film transistor array according to claim 1, wherein said light shield film is formed of a metal oxide.

4. A liquid crystal device, comprising:

a single first substrate;

a plurality of thin film transistors formed on said single first substrate, each thin film transistor having at least a gate electrode, a semiconductor layer having a channel portion, a source electrode and a drain electrode;

a plurality of gate lines and a plurality of drain lines provided over said single first substrate in an intersecting relation via an insulating layer, said gate lines and drain lines being connected to gate and drain electrodes of the transistors at locations near the respective intersections of the gate and drain lines;

a plurality of transparent electrodes electrically connected to the source electrodes and providing a matrix array arranged in a plurality of regions surrounded with the gate and drain lines, respectively;

a transparent insulating film formed at least on said thin film transistors, said gate lines and said drain lines, said transparent insulating film having a first surface which is in contact at least with said thin

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film transistors and said gate and drain lines, and a second surface which is an opposite surface opposing said first surface; and

a single light shield film formed on said second surface of said transparent insulating film, said single light shield film being provided over said single first substrate so as to cover the channel portions of said transistors, said gate lines, and said drain lines, and said single light shield film having a width which is not less than an interval between adjacent peripheral edges of said plurality of transparent electrodes so as to overlap the edges of said plurality of transparent electrodes, to thereby shield said channel portion from light and to shut off light leaking from among a plurality of transparent electrodes;

a second substrate having an opposite electrode arranged opposite to said plurality of transparent electrodes, said second substrate being joined to said single first substrate by a sealing material with a predetermined space between said single first substrate and said second substrate; and

a liquid crystal material sealed in said predetermined space in an area surrounded by said single first substrate, said second substrate and said sealing material.

5. A thin film transistor array, comprising:

a single substrate;

a plurality of thin film transistors formed on said single substrate, each thin film transistor having at least a gate electrode, a semiconductor layer having a channel portion and a source electrode, and a drain electrode;

a plurality of gate lines and a plurality of drain lines provided over said single substrate in an intersecting relation via an insulating film, said gate lines and drain lines being connected to gate and drain electrodes of the transistors at locations near the respective intersections of the gate and drain lines;

a plurality of transparent electrodes electrically connected to the source electrodes and providing a matrix array arranged in a plurality of regions surrounded with the gate and drain lines, respectively;

a transparent insulating film formed at least on said thin film transistor, said gate lines and said drain lines, said transparent insulating film having a first surface which is in contact at least with said thin film transistors and said gate and drain lines, and a second surface which is an opposite surface opposing said first surface; and

a single light shield film formed on said second surface of said transparent insulating film, said single light shield film being over said single substrate so as to cover the channel portions of said transistors, said gate lines, and said drain lines, and said single light shield film having a width which is substantially equal to an interval between adjacent peripheral edges of said plurality of transparent electrodes, so as to overlap the edges of said plurality of transparent electrodes, to thereby shield said channel portions from light and to shut off light leaking from among a plurality of transparent electrodes.

6. A liquid crystal device, comprising:

a single first substrate;

a plurality of thin film transistors formed on said single substrate, each thin film transistor having at least a gate electrode, a semiconductor layer hav-

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ing a channel portion and a source electrode, and a drain electrode;

a plurality of gate lines and a plurality of drain lines provided over said single first substrate in an intersecting relation via an insulating layer, said gate lines and drain lines being connected to gate and drain electrodes of the transistors at locations near the respective intersections of the gate and drain lines;

a plurality of transparent electrodes electrically connected to the source electrodes and providing a matrix array arranged in a plurality of regions surrounded with the gate and drain lines, respectively;

a transparent insulating film formed at least one said thin film transistor, said gate lines and said drain lines, said transparent insulating film having a first surface which is in contact at least with said thin film transistors and said gate and drain lines, and a second surface which is an opposite surface opposing said first surface; and

a single light shield film formed on said second surface of said transparent insulating film, said single light shield film being over said single first substrate so as to cover the channel portions of said transistors, said gate lines, and said drain lines, and said single light shield film having a width which is

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substantially equal to an interval between adjacent peripheral edges of said plurality of transparent electrodes, so as to overlap the edges of said plurality of transparent electrodes, to thereby shield said channel portions from light and to shut off light leaking from among a plurality of transparent electrodes;

a second substrate having an opposite electrode arranged opposite to said plurality of transparent electrodes, said second substrate being joined to said single first substrate by a sealing material with a predetermined space between said single first substrate and said second substrate; and

a liquid crystal material sealed in said predetermined space in an area surrounded by said single first substrate, said second substrate and said sealing material.

7. A thin film transistor array according to claim 1, wherein said single light shield film has a width which is larger than an interval between adjacent peripheral edges of said plurality of transparent electrodes.

8. A liquid crystal device according to claim 4, wherein said single light shield film has a width which is larger than an interval between adjacent peripheral edges of said plurality of transparent electrodes.

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(54) Thin-film transistor and method of manufacturing the same

Dünnschichttransistor und dessen Herstellungsmethode

Transistor à couches minces et sa méthode de fabrication

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Description

The present invention relates to a thin-film transistor panel and a method of manufacturing same according to the preamble parts of claims 1 and 6.

Such a thin-film transistor panel is known for example from JP-A-61164267.

Known as a thin-film transistor for use as, for example, one of the active elements of an active matrix liquid-crystal display is one having an inverse stagger structure. The thin-film transistor of this type comprises a substrate, a gate electrode formed on the substrate, a gate-insulating film formed on the gate electrode, an i-type semiconductor layer formed on the gate-insulating film, an n-type semiconductor layer formed on the i-type semiconductor layer, a source electrode formed on one end portion of the n-type semiconductor layer, a drain electrode formed on the other end portion of the n-type semiconductor layer.

The method which is commonly employed to manufacture a thin-film transistor having the inverse stagger structure will be described, with reference to Figs. 9A to 9E.

Figs. 9A to 9E are cross-sectional views explaining the method of manufacturing the conventional thin-film transistor, which is formed on one of the transparent substrates of an active matrix liquid-crystal display and used as an active element for a pixel electrode.

[Step 1]

First, as is shown in Fig. 9A, a gate electrode 2G is formed on a transparent substrate 1 made of insulative material such as glass. Next, a wiring or a scanning line (not shown) is formed on the substrate 1, which is connected to the gate electrode 2G. A gate-insulating film 3 is formed on the substrate 1, the gate electrode 2G and the scanning line. Further, an i-type semiconductor layer 4 is formed on the gate-insulating film 3, and a blocking insulation layer 7 is formed on the i-type semiconductor layer 4, protecting the layer 4.

The gate electrode 2G and the scanning line (not shown) are formed by depositing Ta, Ta-Mo alloy, Cr, or the like on the substrate 1 by means of sputtering or plating, and then by patterning the resultant metal layer by means of photolithography.

In most cases, the gate-insulating film 3 is made of SiN (silicon nitride) or the like, the i-type semiconductor layer 4 is made of a-Si (amorphous silicon), and the blocking insulation layer 7 is made of the same insulative material (SiN or the like) as the gate-insulating film 3. The film 3, the layer 4, and the layer 7 are continuously formed by plasma CVD method.

[Step 2]

Next, as is shown in Figs. 9B, the blocking insulation layer 7 is patterned by photolithography, to be substan-

tially the same size and shape as that portion of the i-type semiconductor layer 4 which will be a channel region. The i-type semiconductor layer 4 is patterned by Photolithography, forming a layer which has a specific shape.

[Step 3]

As is shown in Fig. 9C, an n-type semiconductor layer 5 is formed by plasma CVD method on the substrate 1, covering the i-type semiconductor layer 4 and the insulation layer 7. A metal film 6, which will be processed to be a source electrode and a drain electrode, is formed on the n-type semiconductor layer 5 by means of sputtering. The n-type semiconductor layer 5 is made of a-Si doped with an impurity, and the metal film 6 is made of Cr or the like.

[Step 4]

Then, as is shown in Fig. 9D, the metal film 6 is patterned by photolithography, forming a source electrode 6S, a drain electrode 6D, and a wiring or a data line (not shown) connected to the drain electrode 6D. Further, the n-type semiconductor layer 5 is etched away, except for those portions which are located beneath the source electrode 6S and the drain electrode 6D to separate the layer 5 at the channel region. As a result, a thin-film transistor is manufactured.

If the n-type semiconductor layer 5 contacts the channel region of the i-type semiconductor layer 4 at the time etching the n-type semiconductor layer 5, the surface of the channel region of the i-type semiconductor layer 4 will also be etched, inevitably damaging the i-type semiconductor layer 4 and degrading the characteristics of the thin-film transistor. In the method described above, the blocking insulation layer 7 is formed on the channel region of the i-type semiconductor layer 4, and the i-type semiconductor layer 4 is therefore prevented from being etched when the n-type semiconductor layer 5 is etched. Hence it is possible to manufacture a thin-film transistor which has good characteristics.

Fig. 9E shows the thin-film transistor thus manufactured and provided with a pixel electrode 8a which is formed on the gate-insulating film 3. The pixel electrode 8a has been by patterning a transparent conductive film made of ITO or the like. The electrode 8a has its one end portion laid on the source electrode 6S, and is thereby electrically connected to the source electrode 6S.

In the prior-art method of manufacturing a thin-film transistor, which has been described above, selective etching is performed on the n-type semiconductor layer 5, thereby removing that portion of this layer 5 which is located above the channel region of the i-type semiconductor layer 4. It is therefore necessary to prevent the i-type semiconductor layer 4 from being etched during the selective etching of the layer 5, so that the i-type semiconductor layer 4 may not be damaged. To this end, the

blocking insulation film 7 must be formed on the channel region of the i-type semiconductor layer 4.

Hence, it is required that the blocking insulation layer 7 be patterned by photolithography, before the n-type semiconductor layer 5 and the metal film 6 are formed. The method inevitably have a large number of steps. This means that the manufacturing cost of the film-film transistor is high if the transistor is made by the conventional method.

To make matter worse, since the blocking insulation layer 7 is made of, as in most cases, the same insulative material (e.g., SiN) as the gate-insulating film 3, the etching solution applied for patterning the layer 7 flows via pinholes made, if any, in the i-type semiconductor layer 4, and reaches the gate-insulating film 3. Thus, the gate-insulating film 3 is inevitably etched, too. Due to such undesired etching of the film 3 which has occurred during the patterning of the blocking insulation layer 7, the gate-insulating film 3 has pin holes. It is through these pin holes that the gate electrode 2G, the source electrode 6S, and the drain electrode 6D are short-circuited.

According to conventional TFTs, the connection terminals of the gate and drain lines are formed of metal and are exposed to the atmospheric air. Therefore the surface regions of the connection terminals are oxidized during the manufacturing process and its usage by oxygen and humidity in the atmosphere. As a consequence thereof, the connection terminals are covered by an insulation oxidation film during the manufacturing process and its usage, thereby resulting in a low reliability.

Accordingly, the object of the present invention is to provide a thin film transistor having a high reliability.

This object is solved by a thin film transistor panel having the features of claim 1 and by a manufacturing method having the steps as set forth in claim 6.

Preferred embodiments are subjects of various dependent claims.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view showing a thin-film transistor array according to a first embodiment of the present invention;

Figs. 2A to 2D are cross-sectional views explaining a method of manufacturing a thin-film transistor;

Fig. 3 is a plan view showing a thin-film transistor panel which incorporates the thin-film transistor shown in Figs. 2A to 2D, and which is a second embodiment of the invention;

Figs. 4 to 6 are cross-sectional views of the thin-film transistor panel, taken along line IV-IV, line V-V, and line VI-VI shown in Fig. 3, respectively;

Figs. 7A to 7D are cross-sectional views explaining how to manufacture the thin-film transistor incorporated in the panel shown in Figs. 4 to 6, and Figs.

8A to 8D are cross-sectional views explaining how to manufacture the thin-film transistor panel; and Figs. 9A to 9E are cross-sectional view explaining a method of manufacturing a conventional thin-film transistor.

A thin-film transistor formed on one of the transparent substrates of an active matrix liquid-crystal display and designed for use as the active element for a pixel electrode, and an array of thin-film transistors of this type (i.e., a TFT array), both being a first embodiment of the present invention, will be described with reference to Fig. 1 and Figs. 2A to 2D.

Fig. 1 is a schematic plan view of the TFT array. As is shown in this figure, the TFT array comprises a substrate 11, a plurality of scanning lines GL formed on the substrate 11 and extending parallel to one another, a plurality of data lines DD extending parallel to one another and at right angles to the scanning lines GL, a plurality of TFT elements 10 arranged in rows and columns, each having its gate electrode connected to one of the scanning line and its drain connected to one of the data lines DL, and a plurality of pixel electrodes 18a arranged in rows and columns and connected to the TFTs, respectively, thus forming a display region.

Each TFT element 10 and each pixel electrode 18a, which are located at the intersection of a scanning line GL and a data line DL, will now be described with reference to Fig. 2D. As is shown in Fig. 2D, the TFT element 10 comprises a gate electrode 12G, a gate-insulating film 13 covering the gate electrode 12G, an i-type semiconductor layer 14 of amorphous silicon formed on that portion of the film 13 which is located above the electrode 12G, an n-type semiconductor layer 15 formed on the i-type layer 14, a drain electrode 16D formed on that portion of the n-type layer 15 which is located on one end portion of the i-type layer 14, and a source electrode 16S formed on that portion of the n-type layer 15 which is located on the other end portion of the i-type layer 14. The gate electrode 12G is integral with one of the scanning lines GL formed on the substrate 11. The drain electrode 16D is connected to an data line DL, and the source electrode 16S is connected to one of the pixel electrodes 18a which are made of transparent conductive film. The i-type semiconductor layer 14 has a channel region which has been anodically oxidized and, thus, functions as an insulative film 15a.

It will now be explained how the TFT 10 is manufactured, with reference to Figs. 2A to 2D.

[Step 1]

First, as is shown in Fig. 2A, a gate electrode 12 is formed on a transparent substrate 11 made of insulative material such as glass. Next, a scanning line GL is formed on the substrate 1, which is connected to the gate electrode 12. A gate-insulating film 13 made of SiN or the like is formed by plasma CVD method on the sub-

strate 11, the gate electrode 12 and the scanning line. Further, an i-type semiconductor layer 14 made of a-Si is formed on the gate-insulating film 13 by means of plasma CVD method. Then, an n-type semiconductor layer 15 made of a-Si doped with an n-type impurity is formed on the i-type semiconductor layer 14 by means of plasma CVD method. Further, a metal film 16 made of metal such as Cr, which will be processed to be a source electrode and a drain electrode, is formed on the n-type semiconductor layer 15 by means of sputtering.

The n-type semiconductor layer 15 is about 25 to 100 nm thick, whereas the metal film 16 is about 200 to 500 nm thick. The gate electrode 12 and the scanning line GL are formed by depositing Ta, Ta-Mo alloy, Cr, Al, Al-Ti alloy or the like on the substrate 11 by means of sputtering or plating, and then by patterning the resultant metal layer by means of photolithography.

[Step 2]

Next, as is shown in Fig. 2B, the metal film 16 is patterned by photolithography, forming a source electrode 16S, a drain electrode 16D, and a data line DL connected to the drain electrode 16D. Thereafter, the n-type semiconductor layer 15 is etched away, except for the portions located beneath the electrodes 16S and 16D and that portion extending between these electrodes 16S and 16D. Also, the i-type semiconductor layer 14 is etched away, except for those portions which are located beneath the electrodes 16S and 16D and that portion which will be a channel region.

This selective etching of the layers 14 and 15 is accomplished by using both the source electrode 16S and the drain electrode 16D as etching masks, and by forming a resist mask (not shown) on those portions of the n-type layer 15 which are located beneath the source electrode 16S and the drain electrode 16D and on that portion of the layer 15 which extends between the electrodes 16S and 16D.

[Step 3]

The resist mask is removed from the n-type semiconductor layer 15. Then, as is shown in Fig. 2C, that portion of the n-type semiconductor layer 15, which extends between the electrodes 16S and 16D and is located on that portion of the i-type semiconductor layer 14 which will be the channel region, is oxidized anodically in its entirety thickness direction. This portion of the layer 15, thus oxidized, electrically cuts the n-type semiconductor layer 15 into two parts. Thus, a thin-film transistor 10 is manufactured.

More specifically, the portion of the n-type semiconductor layer 15 is anodically oxidized in the following way. First, the wiring (hereinafter referred as a data line) extending from the drain electrode 16D is connected to the anode of an DC power supply by a clip-type connector. The unfinished product is immersed in a bath of an

electrolytic solution (e.g., solution of ammonium borate), except for that end of the data line which is connected to the DC power supply. In the solution bath, the unfinished product is so positioned that the drain electrode 16D opposes an opposite electrode (cathode) placed in the solution bath. In this condition, an electric current is supplied to the n-type semiconductor layer 15 through the data line and the drain electrode 16D. A voltage is thereby applied between the layer 15 and the cathode, achieving the anodic oxidation of the n-type semiconductor layer 15. During this anodic oxidation, that portion of the source electrode 16S is kept covered with a resist mask 22.

When the voltage is applied between the n-type semiconductor layer 15 and the cathode, that portion of the layer 15 acting as anode which is immersed in the electrolytic solution (i.e., the portion extending between the source electrode 16S and the drain electrode 16D) undergoes a chemical reaction and is gradually oxidized from its surface. Upon lapse of a predetermined time, said portion of the n-type semiconductor layer 15 changes into an oxidized insulative layer 15a. The layer 15a electrically cuts the n-type semiconductor layer 15 into two parts.

Once anodically oxidized in its entirety thickness direction as described above, that portion of the n-type semiconductor layer 15 which extends between the electrodes 16S and 16D becomes electrically insulative, whereby the n-type semiconductor layer 15 is electrically cut into two parts.

As the n-type semiconductor layer 15 is anodically oxidized gradually from its exposed surface, whereby the oxidized insulation layer 15a grows thicker, said portion of the layer 15 becomes thinner. Nonetheless, the electric current keeps flowing through the n-type semiconductor layer 15 until the insulation layer 15a grows to reach the surface of the i-type semiconductor layer 14. Hence, that portion of the layer 15 can be anodically oxidized in its entirety thickness direction when the current stops flowing through it, only if the voltage applied is relatively high (for example, about 50V in the case where the layer 15 is 25 nm thick). Thus, that portion of the layer 15 which extends between the electrodes 16S and 16D is oxidized in its entirety. In other words, it is oxidized until the current stops flowing at the interface between the i-type semiconductor layer 14 and the n-type semiconductor layer 15. As a result, the n-type semiconductor layer 15 is electrically cut into two parts, at the position above that portion of the i-type semiconductor layer 14 which functions as a channel region.

In this embodiment, the anodic oxidation of said portion of the layer 15 is carried out by supplying an electric current to the n-type semiconductor layer 15 through the data line and the drain electrode 16D. Hence, the surfaces of the data line and the drain electrode 16D also undergo chemical reaction in the electrolytic solution bath and are oxidized anodically. In addition, since the electric current is supplied to the source electrode

16S, too, through the n-type semiconductor layer 15, the source electrode 16S is also anodically oxidized at its upper surface. As a result, as is shown in Fig. 2C, the surfaces of the source electrode 16S and the drain electrode 16D form two oxidized insulation layers 16a. These insulation layers 16a protect the source electrode 16S and the drain electrode 16D, respectively.

Any metal is oxidized faster than any n-type semiconductor under the same condition. Therefore, the oxidized insulation layers 16a grows somewhat thicker than the n-type semiconductor layer 15, while said portion of the layer 15 is being oxidized in its entirety thickness direction. The insulation layer 16a on the source electrode 16S is thinner than the insulation layer 16a formed on the drain electrode 16D for two reasons. First, the voltage applied on the source electrode 16S is one dropped in the n-type semiconductor layer 15. Secondly, no voltage is applied to the source electrode 16S once the n-type semiconductor layer 15 has been electrically cut into to parts.

Although the oxidized insulation layers 16a are somewhat thicker than the n-type semiconductor layer 15, both the source electrode 16S and the drain electrode 16D remain thick enough to attain sufficient conductivity. This is because, as has been pointed out, these electrodes 16S and 16D have a thickness of about 200 to 500 nm, far greater than the thickness (i.e., about 25 to 100 nm) of the n-type semiconductor layer 15 before their surfaces are oxidized anodically.

The thin-film transistor, thus manufactured, is used as one of active elements of an active matrix liquid-crystal display. Therefore, its source electrode 16S needs to be electrically connected at an end to a pixel electrode. The end portion of the source electrode 16S will not be electrically connected to the pixel electrode if the surface of this end portion is oxidized anodically. To prevent such an electrical disconnection, the end portion of the electrode 16S is covered with a resist mask 22 as is shown in Fig. 2C before the anodic oxidation is carried out. Since the mask 22 protects the end portion of the electrode 16S from the electrolytic solution, the end portion of the electrode 16S is electrically connected to the pixel electrode, achieving good conduction between the source electrode 16S and the pixel electrode.

As is shown in Fig. 2D, a pixel electrode 18a is formed on a portion of the gate-insulating film 13. The pixel electrode 18a has a portion formed on one portion of the source electrode 16S of the thin-film transistor. The electrode 18a is made by removing the resist mask 22 from the end portion of the electrode 16S, forming a transparent conductive film made of ITO or the like on the end portion of the electrode 16S, and patterning the conductive film thus formed.

In the method of manufacturing a thin-film transistor, described above, the n-type semiconductor layer 15 is electrically cut at the portion located above the channel region of the transistor, not by means of etching but by means of anodic oxidation. More precisely, that por-

tion of the layer 15 becomes electrically insulative when it is anodically oxidized in its entirety thickness direction, whereby the n-type semiconductor layer 15 is electrically cut into two parts.

Since the n-type semiconductor layer 15 is electrically divided into two parts not by etching, a blocking insulation film need not be formed on the channel region of the i-type semiconductor layer 14 as in the prior-art method. Hence, no damages are done to the i-type semiconductor layer 14 during the manufacture of the thin-film transistor. Without a step of forming a blocking insulation film, the method of the present invention helps to reduce the cost of manufacturing thin-film transistors.

Since no blocking insulation film needs to be formed in the method described above, pinholes are not formed in a gate-insulating film as in the conventional method of manufacturing a thin-film transistor. Thus there is no possibility that the gate electrode 12 is short-circuited with the source electrode 16S or the drain electrode 16D. With this method it is therefore possible to enhance the yield of thin-film transistors.

In the first embodiment, the surface of the source electrode 16S and that of the drain electrode 16D are oxidized at the time of anodically oxidizing the selected portion of the n-type semiconductor layer 15. Instead, only that portion of the layer 15 can be anodically oxidized, with both the source electrode 16S and the drain electrode 16D covered with resist masks.

The method described above, which is the first embodiment of the invention is one for manufacturing a thin-film transistor which is formed on one of the two transparent substrates of an active matrix liquid-crystal display and which is designed as the active element for a pixel electrode. Nonetheless, the method can be used to manufacture a thin-film transistor for any other purpose.

As has been described, in the method the n-type semiconductor layer is electrically divided into two parts at the portion located above the channel region of the thin-film transistor, not by means of etching but by anodic oxidation. Thus, no damages are done to the i-type semiconductor layer located beneath the n-type semiconductor layer. The method, therefore, has no step of forming a blocking insulation layer, making it possible to manufacture the thin-film transistor at low cost. In addition, there is no possibility that pinholes are formed in the gate-insulating film to cause short-circuiting of the gate electrode, the source electrode or the drain electrode, making it possible to enhance the yield of thin-film transistors.

The advantages pointed out in the preceding paragraph, can be attained by the other methods to be described below.

The thin-film transistor according to the invention, and the method of manufacturing this invention will be described, with reference to Figs. 3 to 7 and Figs. 8A to 8D. The components which are identical or similar to those shown in Figs. 2A to 2D will be designated at the

same reference numerals and will not be described in detail.

First, the construction of the thin-film transistor will be described. Fig. 3 is a plan view showing a part of a thin-film transistor (TFT) panel which incorporates the thin-film transistor. Figs. 4, 5, and 6 are cross-sectional views of the TFT panel, taken along line IV-IV, line V-V, and line VI-VI shown in Fig. 3, respectively;

The TFT panel comprises a transparent substrate 11 made of glass or the like, pixel electrodes 18a formed on the substrate 11, and thin-film transistor elements 10 formed on the substrate 11 and functioning as active elements for the electrodes 18a.

As can be understood from Figs. 3 and 4, the thin-film transistor element 10 comprises a gate electrode 12G formed on the substrate 11, a gate-insulating film 13 covering the gate electrode 12G, an i-type semiconductor layer 14 formed on a portion of the gate-insulating film 13, an n-type semiconductor layer 15 formed on the i-type semiconductor layer 14, a contact layer 19 formed on the n-type semiconductor layer 15, and a source electrode 16S formed on the contact layer 19, and a drain electrode 16D formed on the contact layer 19. The contact layer 19 is made of metal such as Cr.

The gate electrode 12G is integral with a gate line GL formed on the substrate 11. The gate-insulating film 13 covers both the gate electrode 12G and the gate line GL, and is formed on almost the entire surface of the substrate 11. The film 13 is made of SiN or the like. Formed on the gate-insulating film 13 is a data line DL which is connected to the drain electrode 16D. The gate electrode 12G and the gate line GL are formed of a gate metal film 12 which is made of aluminum or an aluminum alloy. The source electrode 16S, the drain electrode 16D, and the data line DL are formed of a drain metal film 16 which is made of aluminum or an aluminum alloy.

The contact layer 19 is divided into two parts, on which the electrode 16S and 16D are formed, respectively. That part of the layer 19 on which the source electrode 16S is formed has substantially the same shape and size as the source electrode 16S. Similarly, that part of the layer 19 on which the drain electrode 16D is formed has substantially the same shape and size as the source electrode 16D.

The n-type semiconductor layer 15 is formed on the entire surface of the i-type semiconductor layer 14. That portion of this layer 15 which is located below the gap between the source electrode 16S and the drain electrode 16D has been oxidized in its entirety thickness direction and is, therefore, an insulation layer 15a. The peripheral portions of both semiconductor layers 14 and 15 extend outward from the electrodes 16S and 16D. That peripheral portion of the n-type semiconductor layer 15 which extends outward from the drain electrode 16D has been oxidized and is, thus, an insulation layer 15a. Although not shown in Fig. 3 or Fig. 4, that peripheral portion of the n-type semiconductor layer 15 which extends outward from the source electrode 16S has

been slightly oxidized.

The pixel electrode 18a is formed on a protective insulation film 17 which is formed on the gate-insulating film 13. The film 17 covers the thin-film transistor element 10, and is made of SiN or the like. The electrode 18a has been formed by patterning a transparent conductive film 18 made of ITO or the like. Its end extends through the contact hole 17a made in the protective insulation film 17 and is thereby electrically connected to the source electrode 16S of the thin-film transistor element 10.

As is shown in Figs. 3 and 5, the terminal portion DLa of the data line DL consists of two layers. The lower layer is a metal film 16 and the upper film is a part of the transparent conductive film 18, the remaining part of which is the pixel electrode 18a. The upper film (i.e., the transparent conductive film) 18 is deposited on the lower layer (i.e., the metal film) 16, in the opening 17b which is made in the gate-insulating film 13 and the protective insulation film 17, respectively.

The terminal portion GLa of the gate line GL consists of two layers, too, as is shown in Figs. 3 and 6. The lower layer is a part of the gate metal film 12, and the upper film is a part of the transparent conductive film 18, the remaining part of which is the pixel electrode 18a. The upper film (i.e., the transparent conductive film) 18 is deposited on the lower film (i.e., the gate metal film) 12, in the openings 13a and 17c which are made in the gate-insulating film 13 and the protective insulation film 17, respectively.

With reference to Figs. 7A to 7D, it will be explained how the thin-film transistor, described above, is manufactured. With reference to Figs. 8A to 8D, it will be explained how the TFT panel incorporating the transistor is manufactured.

Figs. 7A to 7D and Figs. 8A to 8D are cross-sectional views, each showing the thin-film transistor section of the FET panel, the terminal portion of the data line of the thin-film transistor, and the terminal portion of the data line thereof.

[Step 1]

First, as is shown in Fig. 7A, the gate electrode 12G and the gate line GL are formed on the substrate 11 made of glass or the like. The electrode 12G and the gate line GL are formed by depositing the gate metal film 12 on the substrate 11 and patterning the film 12 by means of photolithography. The metal film 12 shown at the upper-right corner of Fig. 7A is the lower film of the terminal portion GLa of the gate line GL.

[Step 2]

As is shown in Fig. 7A, too, the gate-insulating film 13 is formed on the substrate 11, covering the gate electrode 12G and the gate line GL. The i-type semiconductor layer 14 is formed on the gate insulating film 13. The

n-type semiconductor layer 15 is formed on the i-type semiconductor layer 14. The contact layer 19 is formed on the n-type semiconductor layer.

[Step 3]

Next, as is shown in Fig. 7B, the contact layer 19, the n-type semiconductor layer 15, and the i-type semiconductor layer 14 are patterned by photolithography, whereby these layers 19, 15, and 14 come to have the shape and size identical to a transistor element region to be formed.

[Step 4]

As is shown in Fig. 7C, the metal film 16, which will be patterned into the source electrode 16S and the drain electrode 16D, is formed on the substrate 11 and on the gate-insulating film 13, covering the layers 14, 15, and 19 which have been patterned.

[Step 5]

As is shown in Fig. 7D, the metal film 16 is patterned by photolithography, forming the source electrode 16S, the drain electrode 16D, and the data line DL (see Fig. 4). Then, using the resist mask 21 which has been used in patterning the metal film 16, the contact layer 19 is patterned into two pieces of film which have the same shape and size as the source electrode 16S and the drain electrode 16D, respectively. The metal film 16 shown in the upper-right corner of Fig. 7D is the lower film of the terminal portion DLa of the data line.

[Step 6]

As shown in Fig. 7D, too, oxidation is performed on the n-type semiconductor layer 15, using the resist mask 21 which has been used in patterning the metal film 16. That portion of the n-type semiconductor layer 15 which extends between the electrodes 16S and 16D is oxidized in its entirety, thickness direction forming an oxidized insulation layer 15a. The insulation layer 15a, thus formed, electrically isolates the two portions of the n-type semiconductor layer 15, on which the source electrode 16S and the drain electrode 16D are respectively formed. Thus is manufactured the thin-film transistor element 10.

The portion of the n-type semiconductor layer 15 may be oxidized in the same way as in the first embodiment.

Through the data line DL and the drain electrode 16D, an electric current is supplied to the n-type semiconductor layer 15 during the anodic oxidation of said portion of the layer 15. Hence, the n-type semiconductor layers 15 of all thin-film transistor elements (in this figure only one element is shown) which are arranged along the data line DL can be anodically oxidized uniformly.

Since the resist mask 21 does not cover neither the sides of the drain electrode 16D nor the sides of the data line DL, the sides of both the electrode 16D and those of the data line DL are oxidized anodically. (The resultant oxide layers are not shown.) Nonetheless, the center portion of the electrode 16D or the center portion of the data line DL is not oxidized at all. Therefore, both the drain electrode 16D and the data line DL maintain as electrically conductive as is desired.

The i-type semiconductor layer 14 and the n-type semiconductor layer 15 extend outward from the peripheries of the electrodes 16S and 16D -- that is, from the periphery of the resist mask 21. Hence, that portions of the layer 15 which extend from the periphery of the drain electrode 16D are oxidized, forming the insulation layers 15a. Also, the surface of that portion of the layer 15 which extends from the source electrode 16S, and the sides of the source electrode 16S are slightly oxidized, though not shown in Figs. 7A to 7D.

The resistivity which the i-type semiconductor layer 14 has when no voltage is applied to the gate electrode 15G is 100 or more times greater than the resistivity of the n-type semiconductor layer 15. Therefore, the i-type semiconductor layer 14, located below the layer 15, is not oxidized at all when the n-type semiconductor layer 15 is oxidized anodically.

The TFT panel is manufactured as will be explained below, after a number of thin-film transistor elements 10 have been formed as has been described above.

[Step 7]

The resist mask 21 is removed. As is shown in Fig. 8A, the protective insulation film 17 is formed on the gate-insulating film 13, thus covering the thin-film transistor elements 10.

[Step 8]

Next, as can be understood from Fig. 8B, the protective insulation film 17 is patterned by means of photolithography, making a contact hole 17a, an opening 17b, and an opening 17c. The hole 17a exposes the source electrode 16S of the transistor element 10; the opening 17b exposes that portion of the metal film 16 which will be connected to the terminal portion DLa of the data line DL; and the opening 17c exposes the gate-insulating film 13. An opening 13a aligned with the opening 17c is formed in the gate-insulating film 13, thus exposing that portion of the metal film 12 which will be connected to the terminal portion GLa of the gate line GL.

Then, as is shown in Fig. 8C, the transparent conductive film 18 made of ITO or the like is formed on the protective insulation film 17, also in the contact holes 17a and the openings 17b and 17c, all made in the film 17, and also in the opening 13a made in the gate-insulating film 13. Therefore, the film 18 is formed on the source electrode 16S of the thin-film transistor element

10, and on the lower films 16 and 12 of the terminal portion DL_a of the data line DL, and of the terminal portion GL_a of the gate line GL (i.e., the metal films 16 and 12).

Further, as is shown in Fig. 8D, the transparent conductive film 18 is patterned by photolithography, forming the pixel electrode 18a, the upper film of the terminal portion DL_a of the data line DL, and the upper film of the terminal portion GL_a of the gate line GL. As a result, the TFT panel is manufactured.

Claims

1. A thin film-transistor panel,

the transistor of which are formed on an insulating substrate (11) and include a source electrode (16S), a drain electrode (16D) and

a gate electrode (12G);

the panel further comprising

a gate line (GL) connected to the gate electrode (12G);

a gate-insulating film (13) covering the gate electrode (12G) and the gate line (GL);

an i-type semiconductor film (14) to face the gate electrode (12G) through the insulating film (13) therebetween;

a first n-type semiconductor film (15) formed on a source region of the i-type semiconductor film (14);

a second n-type semiconductor film (15) formed on a drain region of the i-type semiconductor film (14);

the source electrode (16S) being electrically connected to the source region of the i-type semiconductor film (14) through the first n-type semiconductor film (15);

the drain electrode (16D) being electrically connected to the drain region of the i-type semiconductor film (14) through the second n-type semiconductor film (15);

a drain line (DL) connected to the drain electrode (16D);

an insulating film (15a) located between the source and drain electrodes to electrically isolate said source and drain electrodes;

a pixel electrode (18a) formed of transparent conductive material and formed on and electrically connected to said source electrode (16S);

a gate connection terminal (GL_a) connected to the gate line (GL); and

a drain connection terminal (DL_a) connected to the drain line (DL);

characterized in that

the gate connection terminal (GL_a) has a lower film (12) of metal and an upper film (18) of transparent conductive material preventing the lower film (12) from being exposed to the atmosphere; and

the drain connection terminal (DL_a) has a lower film (16) of metal and an upper film (13) of transparent conductive material preventing the lower film (16) from being exposed to the atmosphere.

2. A thin-film transistor panel according to claim 1, characterized in that the transparent conductive material is formed of ITO.

3. A thin-film transistor panel according to claim 1 or 2 characterized by further comprising a protective insulating film (17) covering said thin-film transistor element (10) and having a first opening (17a) located on said source electrode (16S), a second opening (17b) located on the drain connection terminal (DL_a) and a third opening (17c) located on the gate connection terminal (GL_a), and said pixel electrode (18a) being formed on the protective film (17) and connected to the source electrode (16S) through the first opening, the upper film of the drain connection terminal (DL_a) extending through the second opening (17b), and the upper film (18) of the gate connection terminal (GL_a) extending through the third opening (17c).

4. A thin film transistor panel according to at least one of at least claims 1 to 3, characterized in that the insulating film (15a) is formed of an oxidized n-type semiconductor film (15).

5. A thin-film transistor panel according to at least one of claims 1 to 4 characterized by further comprising a first contact film (19) formed between the source electrode (16S) and the first n-type semiconductor film (15), and a second contact film (19) formed between the drain electrode (16D) and the second n-type semiconductor film (15).

6. A method of manufacturing a thin-film transistor

panel having TFT elements arranged in a matrix form comprising the steps of:

forming a TFT element having a gate electrode (12G), a gate line (GL) connected to the gate electrode (12G) and having a metal film (12), a gate-insulating film (13) formed on the gate electrode (12G) and the gate line (GL), an i-type semiconductor film (14) formed on the gate-insulating film (13), a source electrode (16S) connected to a source region of the i-type semiconductor film (14) through an n-type semiconductor film (15), a drain electrode (16D) connected to a drain region of the i-type semiconductor film (14) through said n-type semiconductor film (15), and insulating film (15a) formed on a channel region of the i-type semiconductor film, and a drain line (DL) connected to the drain electrode (16D) and a metal film (16), and

forming a pixel electrode (18a) made of a transparent conductive film (18) on the TFT element

characterized in that
the pixel electrode forming step includes the steps of forming a transparent conductive film (13) on the TFT element (10) and the metal films (12,16) and patterning the transparent conductive film (18) so as to form the pixel electrode (13a) connected to the source electrode (16S) and to form connection terminals (DLa,GLa) formed on the metal films (12,16) of the drain and gate lines (DL,GL).

7. The method according to claim 5, characterized by further comprising a step of forming a contact film (19) on the n-type semiconductor film (14), and in that the step of patterning the n-type semiconductor films also patterns the contact film (19) into the element shape.

Patentansprüche

1. Dünnschicht-Transistorplatte, deren Transistoren auf einem isolierenden Substrat (11) gebildet sind und eine Sourceelektrode (16S), eine Drainelektrode (16D) und eine Gateelektrode (12G) einschließen, wobei die Platte weiter umfaßt:

eine Gateleitung (GL), die mit der Gateelektrode (12G) verbunden ist;

einen Gate-Isolierfilm (13), der die Gateelektrode (12G) und die Gateleitung (GL) bedeckt;

einen I-Typ-Halbleiterfilm (14), der der Gateelektrode (12G) über den Isolierfilm (13) dazwi-

schen gegenüberliegt;

einen ersten N-Typ-Halbleiterfilm (15), der auf einer Sourcezone des I-Typ-Halbleiterfilms (14) gebildet ist;

einen zweiten N-Typ-Halbleiterfilm (15), der auf einer Drainzone des I-Typ-Halbleiterfilms (14) gebildet ist,

wobei die Sourceelektrode (16S) über den ersten N-Typ-Halbleiterfilm (15) mit der Sourcezone des I-Typ-Halbleiterfilms (14) elektrisch verbunden ist,

wobei die Drainelektrode (16D) über den zweiten N-Typ-Halbleiterfilm (15) mit der Drainzone des I-Typ-Halbleiterfilms (14) elektrisch verbunden ist,

eine Drainleitung (DL), die mit der Drainelektrode (16D) verbunden ist;

einen Isolierfilm (15a), der zwischen der Source- und der Drainelektrode gelegen ist und die Source- und die Drainelektrode elektrisch isoliert;

eine Pixelelektrode (18a), die aus durchsichtigem leitfähigem Material gebildet ist und auf der Sourceelektrode (16S) gebildet und damit elektrisch verbunden ist;

einen Gate-Verbindungsanschluß (GLa), der mit der Gateleitung (GL) verbunden ist, und

einen Drain-Verbindungsanschluß (DLa), der mit der Drainleitung (DL) verbunden ist,

dadurch gekennzeichnet, daß

der Gate-Verbindungsanschluß (GLa) einen unteren Film (12) aus Metall und einen oberen Film (18) aus durchsichtigem leitfähigem Material aufweist, der verhindert, daß der untere Film (12) der Atmosphäre ausgesetzt wird, und

der Drain-Verbindungsanschluß (DLa) einen unteren Film (16) aus Metall und einen oberen Film (18) aus durchsichtigem leitfähigem Material aufweist, der verhindert, daß der untere Film (16) der Atmosphäre ausgesetzt wird.

2. Dünnschicht-Transistorplatte nach Anspruch 1, dadurch gekennzeichnet, daß das durchsichtige leitfähige Material aus ITO gebildet ist.

3. Dünnschicht-Transistorplatte nach Anspruch 1

- oder 2, dadurch gekennzeichnet, daß sie weiter einen Schutzisolierfilm (17) umfaßt, der das Dünnschicht-Transistorelement (10) bedeckt und eine erste Öffnung (17a), die auf der Sourceelektrode (16S) gelegen ist, eine zweite Öffnung (17b), die auf dem Drain-Verbindungsanschluß (DLa) gelegen ist, und eine dritte Öffnung (17c) aufweist, die auf dem Gate-Verbindungsanschluß (GLa) gelegen ist, und wobei die Pixelelektrode (18A) auf dem Schutzfilm (17) gebildet und durch die erste Öffnung mit der Sourceelektrode (16S) verbunden ist, der obere Film des Drain-Verbindungsanschlusses (DLa) sich durch die zweite Öffnung (17b) erstreckt und der obere Film (18) des Gate-Verbindungsanschlusses (GLa) sich durch die dritte Öffnung (17c) erstreckt.
4. Dünnschicht-Transistorplatte nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß der Isolierfilm (15a) aus einem oxidierten N-Typ-Halbleiterfilm (15) gebildet ist.
5. Dünnschicht-Transistorplatte nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß sie weiter einen ersten zwischen der Sourceelektrode (16S) und dem ersten N-Typ-Halbleiterfilm (15) gebildeten Kontaktfilm (19), und einen zweiten zwischen der Drainelektrode (16D) und dem zweiten N-Typ-Halbleiterfilm (15) gebildeten Kontaktfilm (19) umfaßt.
6. Verfahren zur Herstellung einer Dünnschicht-Transistorplatte mit in einer Matrixform angeordneten TFT-Elementen, das die Schritte umfaßt:
- Bilden eines TFT-Elements mit einer Gateelektrode (12G), einer Gateleitung (GL), die mit der Gateelektrode (12G) verbunden ist und einen Metallfilm (12) aufweist, einem Gate-Isolierfilm (13), der auf der Gateelektrode (12G) und der Gateleitung (GL) gebildet ist, einem I-Typ-Halbleiterfilm (14), der auf dem Gate-Isolierfilm (13) gebildet ist, einer Sourceelektrode (16S), die über einen N-Typ-Halbleiterfilm (15) mit einer Sourcezone des I-Typ-Halbleiterfilms (14) verbunden ist, einer Drainelektrode (16D), die über den N-Typ-Halbleiterfilm (15) mit einer Drainzone des I-Typ-Halbleiterfilms (14) verbunden ist, einem Isolierfilm (15a), der auf einer Kanalzone des I-Typ-Halbleiterfilms (14) gebildet ist, und einer Drainleitung (DL), die mit der Drainelektrode (16D) verbunden ist und einen Metallfilm (16) besitzt, und
- Bilden einer aus einem durchsichtigen leitfähigen Film (18) bestehenden Pixelelektrode (18a) auf dem TFT-Element

dadurch gekennzeichnet, daß der Pixelelektroden-Bildungsschritt die Schritte zum Bilden eines durchsichtigen leitfähigen Films (18) auf dem TFT-Element (10) und den Metallfilmen (12, 16) und Mustern des durchsichtigen leitfähigen Films (18) umfaßt, um die mit der Sourceelektrode (16S) verbundene Pixelelektrode (18a) und auf den Metallfilmen (12, 16) der Drain- und Gateleitungen (DL, GL) gebildete Verbindungsanschlüsse (DLa, GLa) zu bilden.

7. Verfahren nach Anspruch 6, dadurch gekennzeichnet, daß es weiter einen Schritt zum Bilden eines Kontaktfilms (19) auf dem N-Typ-Halbleiterfilm (15) umfaßt und dadurch, daß der Schritt, der die N-Typ-halbleiterfilme mustert, auch den Kontaktfilm (19) in die Elementform mustert.

Revendications

1. Panneau de transistors à couches minces dont les transistors sont formés sur un substrat isolant (11) et comprennent une électrode de source (16S), une électrode de drain (16D) et une électrode de grille (12G),

le panneau comprenant en outre:

- une ligne de grille (GL) connectée à l'électrode de grille (12G);
- une couche isolante de grille (13) recouvrant l'électrode de grille (12G) et la ligne de grille (GL);
- une couche de semiconducteur du type I (14) faisant face à l'électrode de grille (12G) à travers la couche isolante (13) disposée entre deux;
- une première couche de semiconducteur du type N (15) formée sur une région de source de la couche de semiconducteur du type I (14);
- une deuxième couche de semiconducteur du type N (15) formée sur une région de drain de la couche de semiconducteur du type I (14),

l'électrode de source (16S) étant connectée électriquement à la région de source de la couche de semiconducteur du type I (14) à travers la première couche de semiconducteur du type N (15), et l'électrode de drain (16D) étant connectée électriquement à la région de drain de la couche de semiconducteur du type I (14) à travers la deuxième couche de semiconducteur du type N (15);

- une ligne de drain (DL) connectée à l'électrode de drain (16D);
- une couche isolante (15a) située entre les électrodes de source et de drain pour isoler électriquement lesdites électrodes de source et de drain;
- une électrode d'élément d'image (18a) constituée d'une matière conductrice transparente et formée sur ladite électrode de source (16S) et connectée à celle-ci;
- une borne de connexion de grille (GLa) connectée à la ligne de grille (GL); et
- une borne de connexion de drain (DLa) connectée à la ligne de drain (DL),

caractérisé en ce que:

- la borne de connexion de grille (GLa) a une couche inférieure (12) de métal et une couche supérieure (18) de matière conductrice transparente empêchant la couche inférieure (12) d'être exposée à l'atmosphère; et
 - la borne de connexion de drain (DLa) a une couche inférieure (16) de métal et une couche supérieure (18) de matière conductrice transparente empêchant la couche inférieure (16) d'être exposée à l'atmosphère.
2. Panneau de transistors à couches minces selon la revendication 1, caractérisé en ce que la matière conductrice transparente est constituée d'oxyde d'étain dopé à l'indium (ITO).
3. Panneau de transistors à couches minces selon la revendication 1 ou 2, caractérisé en ce qu'il comprend en outre une couche isolante de protection (17) recouvrant ledit élément à transistor à couches minces (10) et ayant une première ouverture (17a) située sur ladite électrode de source (16S), une deuxième ouverture (17b) située sur la borne de connexion de drain (DLa) et une troisième ouverture (17c) située sur la borne de connexion de grille (GLa); et
- ladite électrode d'élément d'image (18a) étant formée sur la couche de protection (17) et connectée à l'électrode de source (16S) dans la première ouverture, la couche supérieure de la borne de connexion de drain (DLa) s'étendant dans la deuxième ouverture (17b), et la couche supérieure (18) de la borne de connexion de grille (GLa) s'étendant dans la troisième ouverture (17c).
4. Panneau de transistors à couches minces selon au moins une des revendications 1 à 3, caractérisé en ce que la couche isolante (15a) est constituée par une couche oxydée de semiconducteur du type N

(15).

5. Panneau de transistors à couches minces selon au moins une des revendications 1 à 4, caractérisé en ce qu'il comprend en outre une première couche de contact (19) formée entre l'électrode de source (16S) et la première couche de semiconducteur du type N (15), et une deuxième couche de contact (19) formée entre l'électrode de drain (16D) et la deuxième couche de semiconducteur du type N (15).
6. Procédé de fabrication d'un panneau de transistors à couches minces ayant des éléments à transistor à couches minces disposés sous la forme d'une matrice, le procédé comprenant les étapes consistant à:

- former un élément à transistor à couche mince ayant une électrode de grille (12G), une ligne de grille (GL) connectée à l'électrode de grille (12G) et ayant une couche métallique (12), une couche isolante de grille (13) formée sur l'électrode de grille (12G) et la ligne de grille (GL), une couche de semiconducteur du type I (14) formée sur la couche isolante de grille (13), une électrode de source (16S) connectée à une région de source de la couche de semiconducteur du type I (14) à travers une couche de semiconducteur du type N (15), une électrode de drain (16D) connectée à une région de drain de la couche de semiconducteur du type I (14) à travers ladite couche de semiconducteur du type N (15), et une couche isolante (15a) formée sur une région de canal de la couche de semiconducteur du type I, et une ligne de drain (DL) connectée à l'électrode de drain (16D), et une couche métallique (16), et
- former une électrode d'élément d'image (18a) constituée par une couche conductrice transparente (18) sur l'élément à transistor à couches minces,

caractérisé en ce que:

- l'étape de formation de l'électrode d'élément d'image comprend les étapes consistant à former une couche conductrice transparente (18) sur l'élément à transistor à couches minces (10) et les couches métalliques (12, 16), et à mettre en forme de motif la couche conductrice transparente (18) de manière à former l'électrode d'élément d'image (18a) connectée à l'électrode de source (16S) et à former des bornes de connexion (DLa, GLa) formées sur les couches métalliques (12, 16) des lignes de drain et de grille (DL, GL).

7. Procédé selon la revendication 6, caractérisé en ce qu'il comprend une étape consistant à former une couche de contact (19) sur la couche de semiconducteur du type N (14), et en ce que l'étape de mise en forme de motif des couches de semiconducteur du type N met également la couche de contact (19) à la forme de l'élément.

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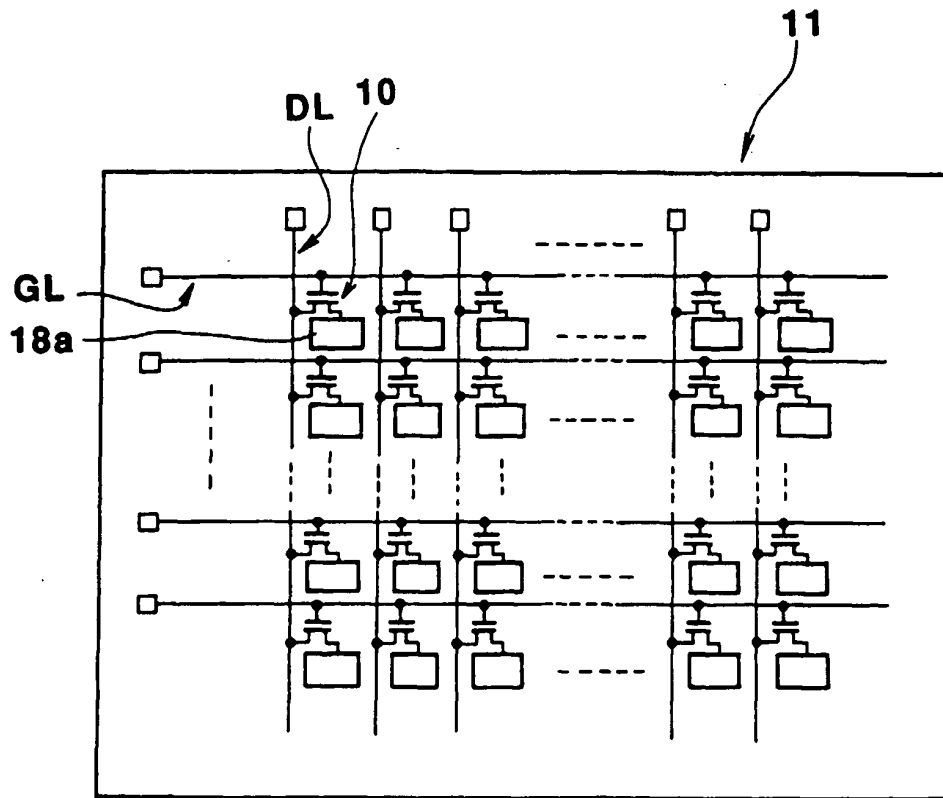


FIG. 1

FIG. 2A

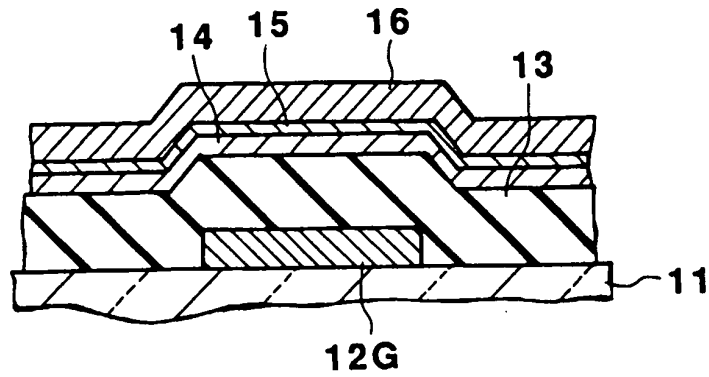


FIG. 2B

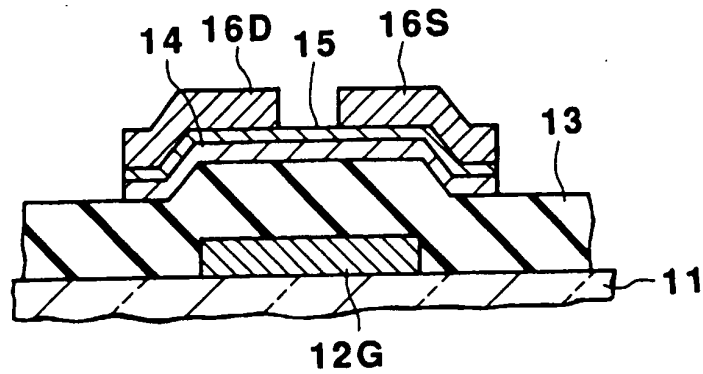


FIG. 2C

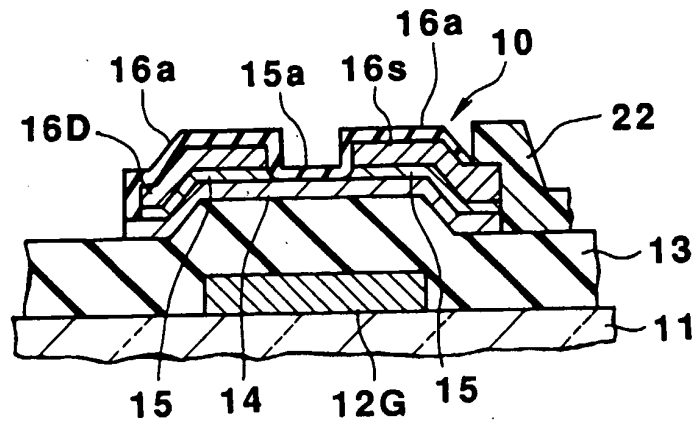
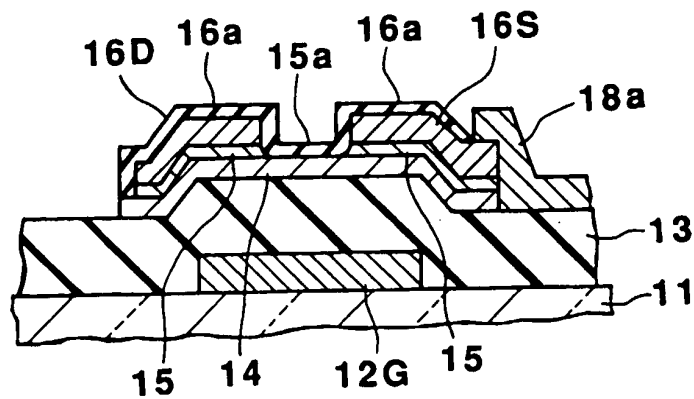


FIG. 2D



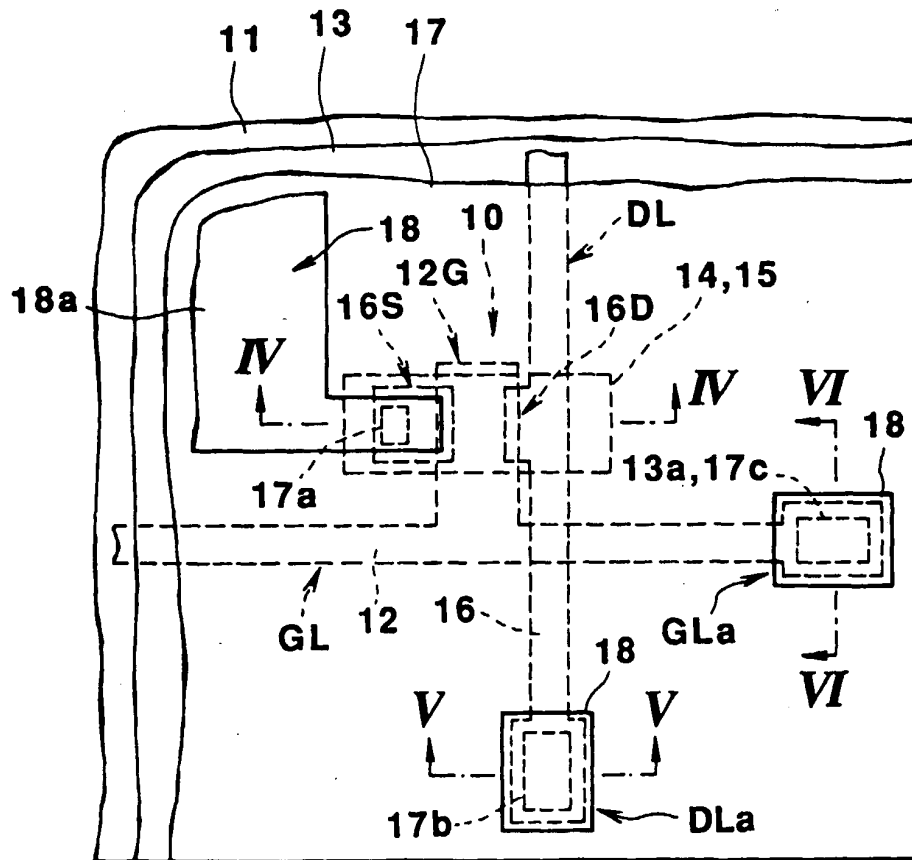


FIG. 3

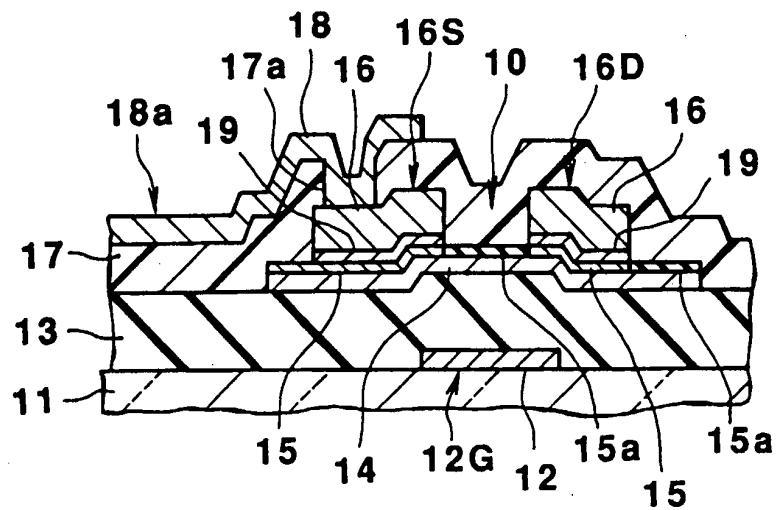


FIG. 4

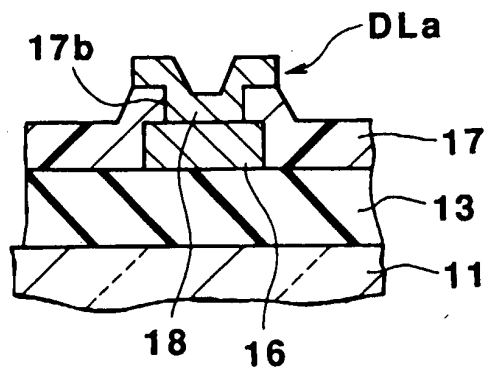


FIG. 5

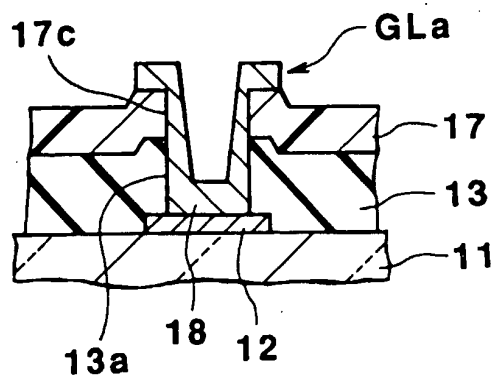


FIG. 6

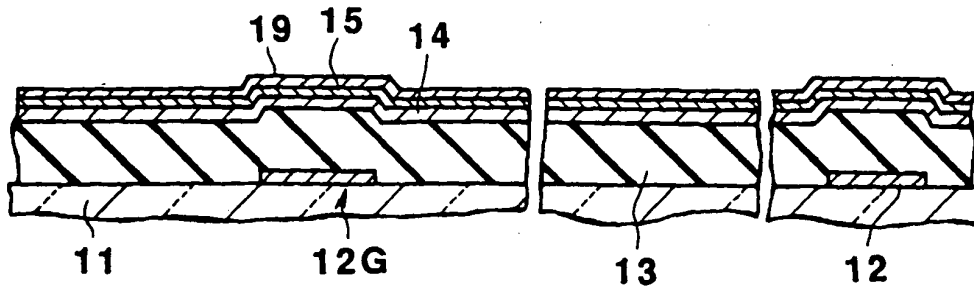


FIG. 7A

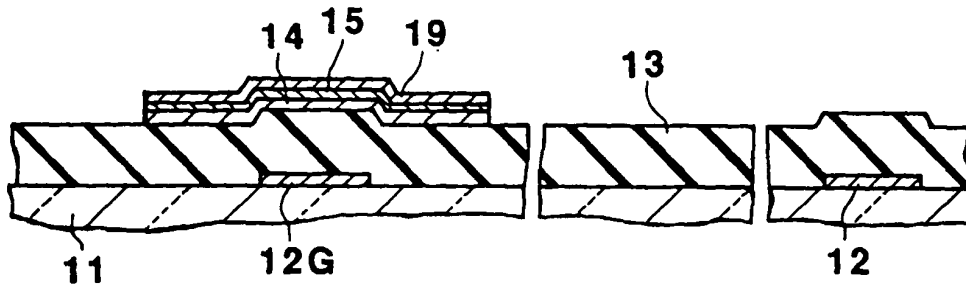


FIG. 7B

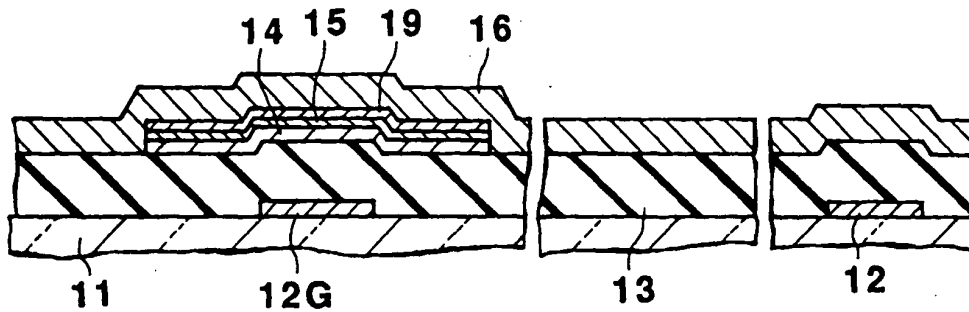


FIG. 7C

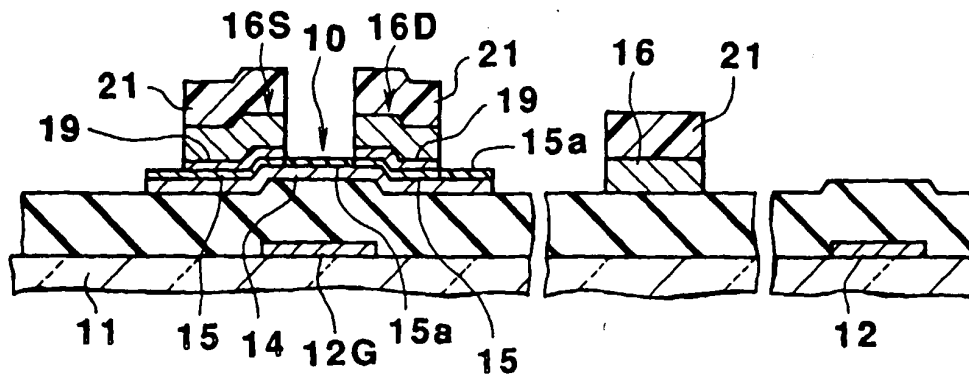


FIG. 7D

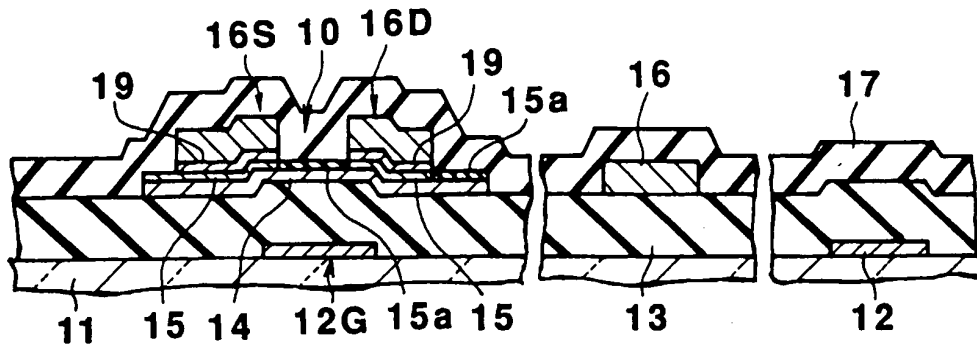


FIG. 8A

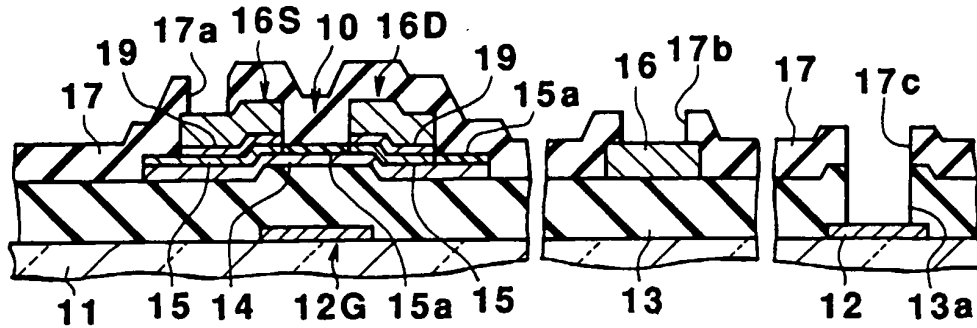


FIG. 8B

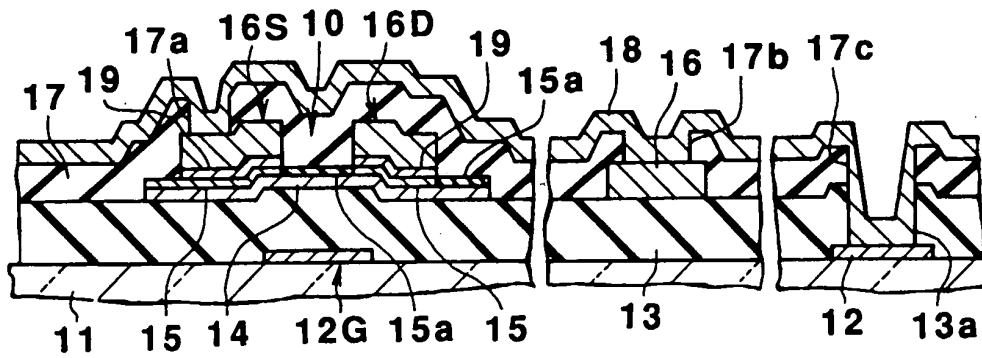


FIG. 8C

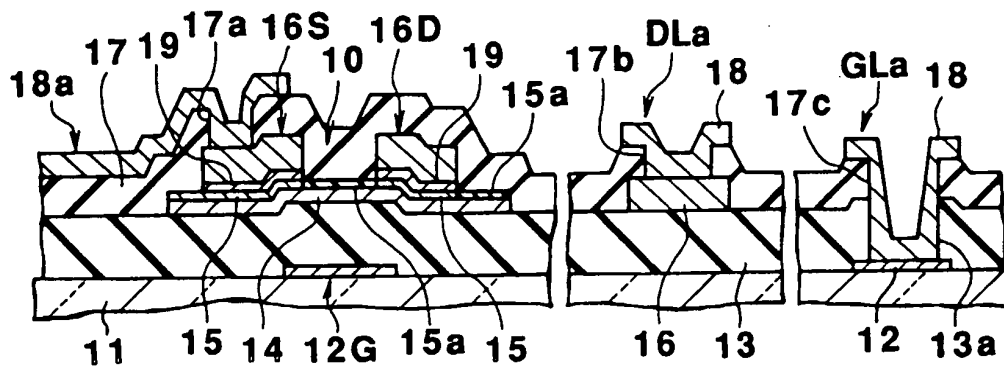


FIG. 8D

FIG. 9A
(PRIOR ART)

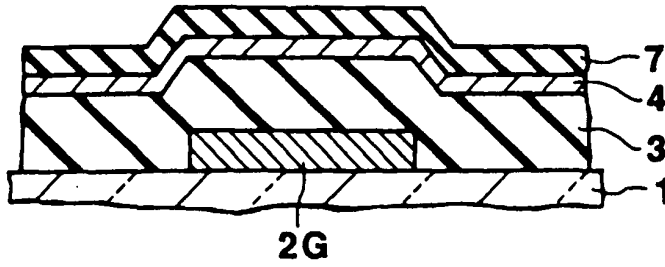


FIG. 9B
(PRIOR ART)

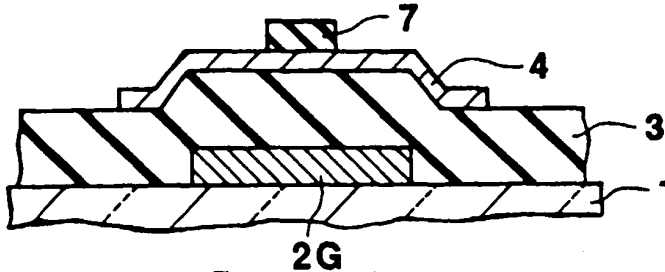


FIG. 9C
(PRIOR ART)

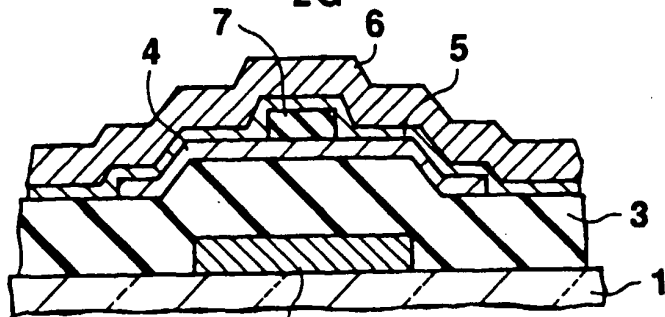


FIG. 9D
(PRIOR ART)

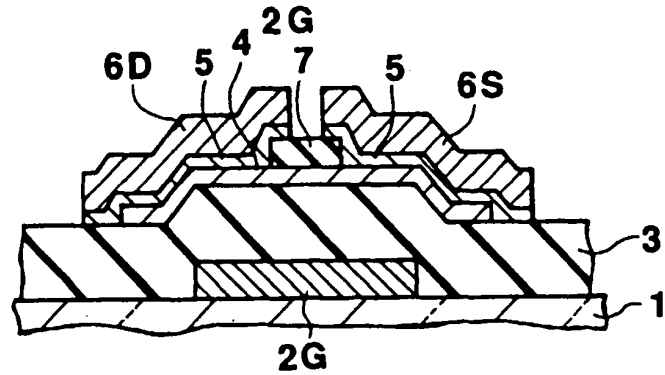


FIG. 9E
(PRIOR ART)

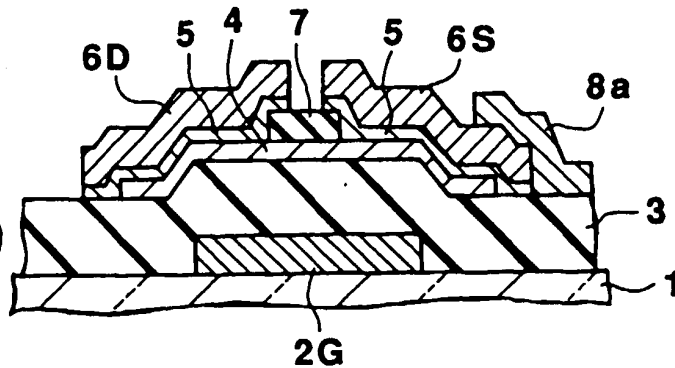


EXHIBIT C-11

Transcript of the Testimony of **Dr. Gary Rubloff**

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L.G. Phillips LCD v. Tatung Co. of America et al

Dr. Gary Rubloff

Page 1

IN THE UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

-----:
 LG. PHILIPS LCD CO., LTD., :
 :
 Plaintiff, :
 :
 vs. :Case No. CV-02-
 : 6775 CBM(JTLx)
 TATUNG CO. OF AMERICA, et al., :
 :Consolidated with
 Defendants. :Case Nos.
 -----:CV 03-2866
 AND CONSOLIDATED CASES :CV 03-2884
 -----:CV 03-2885
 CHUNGHWA PICTURE TUBES, LTD., :CV 03-2886
 :
 Counterclaimant and :
 Third-Party Plaintiff, :
 :
 LG. PHILIPS LCD CO., LTD., :
 :
 Counterdefendant, :
 :
 AND LG ELECTRONICS, INC., :
 :
 Third-Party Defendant.:
 -----:

Washington, D.C.

Thursday, October 27, 2005

Videotaped Deposition of: GARY RUBLOFF, PH.D.

 DIGITAL EVIDENCE GROUP
 11 Dupont Circle, NW Suite 400
 Washington, DC 20036
 (202) 232-0646

10/27/2005

L.G. Phillips LCD v. Tatung Co. of America et al

Dr. Gary Rubloff

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|---|---|
| <p style="text-align: right;">Page 2</p> <p>1 called for oral examination by counsel for 2 Defendants, Counterclaimant and Third-Party 3 Plaintiff, pursuant to notice, at Morgan, Lewis 4 & Bockius, LLP, 1111 Pennsylvania Avenue, Northwest, 5 Washington, D.C., before Shari R. Broussard, a 6 Notary Public in and for the District of Columbia, 7 beginning at 8:59 a.m., when were present on behalf 8 of the respective parties: 9 10 11 12 13 14 15 16 17 18 19 20 21 22</p> | <p style="text-align: right;">Page 4</p> <p style="text-align: center;">C O N T E N T S</p> <p>2 EXAMINATION BY: PAGE 3 Counsel for Defendant, Counterclaimant and Third-Party Plaintiff 7 4 Counsel for Plaintiff/Counterdefendant 319 5 6 7 RUBLOFF DEPOSITION EXHIBITS: * PAGE 8 1 Expert Report 9 9 2 Rebuttal Expert Report 9 10 3 U.S. Patent Number 4,624,737 10 11 4 U.S. Patent Number 5,825,449 10 12 5 Document Labeled Exhibit 17 11 13 6 Document Labeled Exhibit 19 12 14 7 Joint Claim Construction Statement 13 15 8 Diagrams, Exhibit 10, Figure 1 to Figure 34 49 16 9 Diagrams, Exhibit 12, Figure 1 with Attachments 65 17 18 10 Document with Tabs A, B and C 75 19 20 11 U.S. Patent Number 5,162,933 166 21 22 12 L.G. Philips Opening Claim Construction Brief 183 21 13 Diagrams, Exhibit 11, Figure 1 to Figure 20 225 22 14 Document with Tabs A, B and C 293</p> |
| <p style="text-align: right;">Page 3</p> <p>1 On behalf of Plaintiff/Counterdefendant: 2 R. TYLER GOODWYN, IV, ESQUIRE 3 Morgan Lewis & Bockius, LLP 4 1111 Pennsylvania Avenue, Northwest Washington, D.C. 20004 (202) 739-5435 5 On behalf of Defendants, Counterclaimant and Third-Party Plaintiff: 6 7 CHRISTOPHER A. MATHEWS, ESQUIRE Howrey, LLP 8 550 South Hope Suite, Suite 1100 Los Angeles, California 90071 (213) 892-1969 9 10 ALSO PRESENT: 11 Jonathan Perry, Video Technician 12 13 14 15 16 17 18 19 20 21 22</p> | <p style="text-align: right;">Page 5</p> <p style="text-align: right;">PAGE</p> <p>1 RUBLOFF DEPOSITION EXHIBITS: * 2 15 "Efforts of the n+ etching process in TFT-LCD fabrication for Mo/Al/Mo 3 data lines" 301 4 16 Drawing 302 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 (*Exhibits retained by counsel for Claimants.)</p> |

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| <p style="text-align: right;">Page 6</p> <p>1 PROCEEDINGS</p> <p>2 VIDEO TECHNICIAN: This is tape number</p> <p>3 one of the videotaped deposition of Dr. Gary</p> <p>4 Rubloff, taken by Chunghwa Picture Tubes, LTD in</p> <p>5 the matter of LG Philips LCD Company, LTD, versus</p> <p>6 Tatung Company of America, et al., in the U.S.</p> <p>7 District Court for the Central District of</p> <p>8 California, Case Number CV-02-6775 CBM.</p> <p>9 This deposition is being held at the</p> <p>10 offices of Morgan, Lewis, 1111 Pennsylvania Avenue,</p> <p>11 Northwest, Washington, D.C.</p> <p>12 Today's date is October 27th, 2005. The</p> <p>13 time on the video screen is currently 8:59 and 53</p> <p>14 seconds a.m.</p> <p>15 My name is Jonathan Perry. I'm the</p> <p>16 videographer from Digital Evidence Group. The</p> <p>17 court reporter is Shari Broussard also with Digital</p> <p>18 Evidence Group.</p> <p>19 Will counsel present please introduce</p> <p>20 themselves and state whom they represent.</p> <p>21 MR. MATHEWS: Chris Mathews of Howrey</p> <p>22 representing Chunghwa Picture Tubes.</p> | <p style="text-align: right;">Page 8</p> <p>1 Q I'm -- today I will -- I will likely</p> <p>2 refer to them as CPT as a shorthand. Do you</p> <p>3 understand what I mean by CPT?</p> <p>4 A Yes.</p> <p>5 Q I'd like to mark -- I'm sorry. You've --</p> <p>6 you've submitted on behalf of LG Philips LCD two</p> <p>7 expert reports on the issues of invalidity and</p> <p>8 infringement relating to U.S. Patents Number</p> <p>9 4,624,737 and 5,825,449?</p> <p>10 A Yes, two reports.</p> <p>11 Q And today when I refer to those two</p> <p>12 patents, I'll refer to them by the last three</p> <p>13 digits.</p> <p>14 A Yes.</p> <p>15 Q You understand what I mean by that?</p> <p>16 A I understand, yes.</p> <p>17 Q For purposes of the videotape we can</p> <p>18 speak at the same time, however for purposes of the</p> <p>19 court reporter we need to not speak at the same</p> <p>20 time, so I will wait until your answer are complete</p> <p>21 before I ask my next question and it's, for the</p> <p>22 court reporter's sanity, it's best if you wait</p> |
| <p style="text-align: right;">Page 7</p> <p>1 MR. GOODWYN: Tyler Goodwyn from Morgan</p> <p>2 Lewis representing LPL.</p> <p>3 VIDEO TECHNICIAN: Okay. I'm still</p> <p>4 getting some interference from a Blackberry, so if</p> <p>5 we could switch them off.</p> <p>6 (Discussion off the record)</p> <p>7 VIDEO TECHNICIAN: Okay. Will the</p> <p>8 reporter swear in the witness, please.</p> <p>9 WHEREUPON,</p> <p>10 GARY RUBLOFF, PH.D.</p> <p>11 called as a witness, and having been first duly</p> <p>12 sworn, was examined and testified as follows:</p> <p>13 EXAMINATION BY COUNSEL FOR DEFENDANT,</p> <p>14 COUNTERCLAIMANT and THIRD-PARTY PLAINTIFF</p> <p>15 BY MR. MATHEWS:</p> <p>16 Q Good morning, Dr. Rubloff.</p> <p>17 A Good morning.</p> <p>18 Q My name is Chris Mathews. I am</p> <p>19 representing Chunghwa Picture Tubes, who is a</p> <p>20 defendant in this patent infringement lawsuit.</p> <p>21 You're aware of Chunghwa Picture Tubes?</p> <p>22 A Yes.</p> | <p style="text-align: right;">Page 9</p> <p>1 until I finish the question before you -- you</p> <p>2 answer.</p> <p>3 I'd like to mark as Exhibit, and this is</p> <p>4 a little -- we have a lot of depositions going on,</p> <p>5 so I think what we'll do today is we'll mark the</p> <p>6 exhibits as Rubloff Exhibit 1.</p> <p>7 MR. GOODWYN: Okay.</p> <p>8 MR. MATHEWS: That may get slightly</p> <p>9 confusing when we talk about exhibits to his expert</p> <p>10 report, but we'll try to work it out today.</p> <p>11 MR. GOODWYN: Okay.</p> <p>12 MR. MATHEWS: So I'd like to mark as</p> <p>13 Rubloff Exhibit 1 the expert report of Gary Rubloff</p> <p>14 on infringement of the '737 and '449 patents.</p> <p>15 (Rubloff Exhibit Number 1</p> <p>16 was marked for identification.)</p> <p>17 MR. MATHEWS: I'd like to mark as</p> <p>18 Exhibit -- as Rubloff Exhibit 2 the rebuttal expert</p> <p>19 report of Dr. Gary Rubloff on the '737 and the '449</p> <p>20 patent.</p> <p>21 (Rubloff Exhibit Number 2</p> <p>22 was marked for identification.)</p> |

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|---|--|
| <p style="text-align: right;">Page 10</p> <p>1 MR. MATHEWS: I'd like to mark as Rubloff 2 Exhibit 3 U.S. Patent Number 4,624,737. 3 (Rubloff Exhibit Number 3 4 was marked for identification.) 5 MR. MATHEWS: And can we mark as Rubloff 6 Exhibit 4 U.S. Patent Number 5,825,449? 7 (Rubloff Exhibit Number 4 8 was marked for identification.) 9 BY MR. MATHEWS: 10 Q Dr. Rubloff, if you would please put 11 Exhibit 4 in front of you. 12 A Yes. 13 Q This is the '449 patent? 14 A Uh-huh. 15 Q You're familiar with this patent? 16 A Yes. 17 Q In the '449 patent can you explain what 18 is meant by a first conductive layer? 19 A Yes. 20 Q Would you do that, please. 21 A I'd like to refer to the -- this is an 22 exhibit which is already in these reports, and I</p> | <p style="text-align: right;">Page 12</p> <p>1 Q And we can mark as Rubloff Exhibit 6, 2 whether you use the one I give you or not, you 3 know, it's up to you -- 4 A They're the same. 5 Q -- is -- what was Exhibit 19 to your 6 opening expert report. 7 (Rubloff Exhibit Number 6 8 was marked for identification.) 9 BY MR. MATHEWS: 10 Q So in your previous answer you -- you 11 indicated you'd like to refer to exhibits in your 12 report. You're -- you're referring to what -- 13 A Yes. 14 Q -- are now marked as Exhibits 5 and 6? 15 A Yes. Let me make sure about that. Yes. 16 Q Okay. 17 A That will do it. Okay. So let's -- 18 let's start with -- oh, I'm sorry. Do we have the 19 joint claim construction included here? 20 Q I don't have that one I don't believe. 21 A Would you like to use my copy of it? 22 Q Was -- was it an exhibit to your report?</p> |
| <p style="text-align: right;">Page 11</p> <p>1 think it will just make it easier for me to answer 2 your questions accurately and hopefully quickly. 3 Q Which exhibit is that, Dr. Rubloff? 4 A This is Exhibit 17, and I have Exhibit 19 5 as well. 6 Q Why don't we mark as Exhibit 5 I believe 7 what was Exhibit 17 to your opening expert report; 8 is that correct? I'm sorry -- not 17. You said 9 17? 10 A I think it was Exhibit 17 for the '737. 11 Q Oh, for the '737, yes. Okay. 12 A Right. 13 Q So we'll mark that as Exhibit -- as 14 Rubloff Exhibit 5. 15 (Rubloff Exhibit Number 5 16 was marked for identification.) 17 THE WITNESS: Yeah, I only want one in 18 front of me. Put these away maybe, huh? 19 MR. GOODWYN: That would be fine, you can 20 put those away. 21 THE WITNESS: Once we get all of them. 22 BY MR. MATHEWS:</p> | <p style="text-align: right;">Page 13</p> <p>1 A Yeah, it was -- I think it was Part C of 2 one of the exhibits. These are stapled a little 3 better. I think I'll just keep these ones. 4 Q Okay. We'll have to -- I don't -- maybe 5 we can mark that one. 6 A Can we use that one? 7 Q Yeah, why don't you hand it to the 8 reporter and the reporter can mark it. 9 (Rubloff Exhibit Number 7 10 was marked for identification.) 11 THE WITNESS: Okay. That's the one I 12 want to keep out. Okay. Can we come back to the 13 question? I'm sorry. 14 BY MR. MATHEWS: 15 Q Yes. The question is can you -- in the 16 '449 patent can you please explain what is meant by 17 a first conductive layer? 18 A Okay. In the '449 the first conductive 19 layer in claim one is defined as a thickness of 20 electrically conductive material. 21 Q Is the first conductive layer a single 22 piece of metal?</p> |

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| Page 14 | Page 16 |
|---|--|
| <p>1 A The -- the first conductive -- there are</p> <p>2 two ways in one -- in which one would look at that</p> <p>3 here. It is separate pieces of metal that are put</p> <p>4 down in the -- in the deposition of the first</p> <p>5 conductive layer material, and if you're talking</p> <p>6 about the deposition, of course you put them all</p> <p>7 down at the same time, so one has to distinguish</p> <p>8 between these carefully.</p> <p>9 Q So in the '449 patent the first</p> <p>10 conductive layer is the layer of metal that's</p> <p>11 deposited directly onto the substrate?</p> <p>12 A The --</p> <p>13 MR. GOODWYN: Objection.</p> <p>14 Mischaracterizes the witness' testimony.</p> <p>15 THE WITNESS: Yes, the -- the -- there</p> <p>16 are -- there are two ways in which one has to</p> <p>17 interpret conductive layer. If one is talking</p> <p>18 about structures, one has to identify which part of</p> <p>19 the structure because 2A, for example, is different</p> <p>20 from 4 is different from 2. So conductive layer</p> <p>21 has to be interpreted in terms of which parts of</p> <p>22 these are done. They happen to be deposited at the</p> | <p>1 lot at the sequence of steps that are carried out</p> <p>2 to deposit the first conductive layer, first</p> <p>3 insulative layer and so on.</p> <p>4 In the '449 one is talking much more</p> <p>5 about structures, and the -- the -- the first</p> <p>6 deposition of metal, what's called the first</p> <p>7 conductive layer in the sense I've just described,</p> <p>8 then gets separated into different structural</p> <p>9 elements, which is really the focus of the '449</p> <p>10 patent. So for the most part if you want to focus</p> <p>11 and talk now about '449, there are separate</p> <p>12 pieces -- separate pieces of that first conductive</p> <p>13 layer which are referred to in the patent as a</p> <p>14 first conductive layer.</p> <p>15 Q In claim ten of the '449 patent --</p> <p>16 A Uh-huh.</p> <p>17 Q -- are the gate electrode and the gate</p> <p>18 pad and the source pad all made of the first</p> <p>19 conductive layer?</p> <p>20 A Yes, yes. They are -- they -- they are</p> <p>21 all made from the metal that was deposited at the</p> <p>22 same time in one step and then they are formed into</p> |
| Page 15 | Page 17 |
| <p>1 same time and patterned using the mask will make</p> <p>2 them isolated from each other.</p> <p>3 BY MR. MATHEWS:</p> <p>4 Q Are you saying that there are some times</p> <p>5 when a piece of metal from the first metal layer is</p> <p>6 not a first conductive layer in the '449 patent?</p> <p>7 A I'm confused by your question. Would you</p> <p>8 rephrase that?</p> <p>9 Q Well, I'm trying to understand. You said</p> <p>10 there were two constructions. I understand the</p> <p>11 construction where you say it's -- the first</p> <p>12 conductive layer is a -- is a layer of metal that's</p> <p>13 placed down -- I don't want to recharacterize your</p> <p>14 testimony improperly.</p> <p>15 You testified that it -- it -- the first</p> <p>16 conductive layer is separate pieces of metal that</p> <p>17 are in the deposition of the first conductive layer</p> <p>18 material?</p> <p>19 A Yes. I think our confusion comes from</p> <p>20 the fact that the '737 and the '449 are looking at</p> <p>21 different issues.</p> <p>22 In the case of the '737 one is looking a</p> | <p>1 separate structures, each of which would be a first</p> <p>2 conductive layer.</p> <p>3 Q So in a finished product, LCD product --</p> <p>4 A Uh-huh.</p> <p>5 Q -- the gate electrode, the gate pad and</p> <p>6 the source pad are not made of a single piece of</p> <p>7 the first conductive layer?</p> <p>8 A Let me make sure about that. That's</p> <p>9 right.</p> <p>10 Q Is that the same for claim 11 of the '449</p> <p>11 patent?</p> <p>12 A Yes, claim 11 says, "Patterning said</p> <p>13 first conductive layer to form a gate electrode, a</p> <p>14 gate pad and a source pad."</p> <p>15 Q Are you familiar with the term "shorting</p> <p>16 ring" as used in connection with --</p> <p>17 A Yes.</p> <p>18 Q -- TFT LCD products?</p> <p>19 A I'm sorry. May I go back for just a</p> <p>20 second? I think you -- I want to make sure we</p> <p>21 didn't have a confusion about what -- could I --</p> <p>22 could you state the previous question again or can</p> |

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| <p style="text-align: right;">Page 18</p> <p>1 somebody read it back for me?</p> <p>2 Q I had asked you whether the gate</p> <p>3 electrode, the gate pad and the source pad are not</p> <p>4 made of a single piece of the first conductive</p> <p>5 layer for claim ten and you said that's right, and</p> <p>6 then I said is that the same for claim 11 of the</p> <p>7 '449 patent.</p> <p>8 A Yeah, and I want to make sure that I've</p> <p>9 distinguished that the gate electrode can include</p> <p>10 the gate pad, so I -- I wasn't sure whether you</p> <p>11 were trying to ask whether they are physically</p> <p>12 separated from each other. The gate pad and the</p> <p>13 gate electrode are contiguous. The electrode can</p> <p>14 include the pad, the line and -- and so on.</p> <p>15 Q But in a finished TFT LCD product --</p> <p>16 A Uh-huh.</p> <p>17 Q -- the source pad would not be made of</p> <p>18 the same piece of metal as the gate electrode and</p> <p>19 the gate pad?</p> <p>20 A I -- I'm sorry. What product are you</p> <p>21 talking to?</p> <p>22 MR. GOODWYN: Objection. Vague.</p> | <p style="text-align: right;">Page 20</p> <p>1 gate electrode?</p> <p>2 A The same piece of --</p> <p>3 MR. GOODWYN: Same objection.</p> <p>4 THE WITNESS: -- metal? I don't</p> <p>5 understand what you're saying.</p> <p>6 BY MR. MATHEWS:</p> <p>7 Q In a deposition process for a TFT array</p> <p>8 --</p> <p>9 A Right.</p> <p>10 Q -- as described in -- as is described in</p> <p>11 the '449 patent --</p> <p>12 A Right.</p> <p>13 Q -- a first conductive layer is deposited</p> <p>14 on the substrate.</p> <p>15 A Uh-huh.</p> <p>16 Q Is that correct?</p> <p>17 A Uh-huh.</p> <p>18 Q And then it is patterned?</p> <p>19 A Uh-huh.</p> <p>20 Q What is it patterned into?</p> <p>21 A It is patterned into separate first</p> <p>22 conductive layer structures.</p> |
| <p style="text-align: right;">Page 19</p> <p>1 BY MR. MATHEWS:</p> <p>2 Q In a TFT LCD array.</p> <p>3 A They're not all made the same. There are</p> <p>4 many ways to make TFT LCD arrays.</p> <p>5 Q Okay. How about in the '449 patent?</p> <p>6 A In the -- so your question is in the '449</p> <p>7 patent --</p> <p>8 Q Yes.</p> <p>9 A -- the structure -- claim 11, 10?</p> <p>10 Q Ten and 11.</p> <p>11 A Yes. The question is?</p> <p>12 Q Are the -- is the source pad connected --</p> <p>13 I'm sorry.</p> <p>14 Is the source pad made of the same piece</p> <p>15 of first conductive layer as the gate pad and the</p> <p>16 gate electrode?</p> <p>17 MR. GOODWYN: Objection.</p> <p>18 THE WITNESS: Is the source pad made</p> <p>19 of -- I'm sorry. Please say it one more time.</p> <p>20 BY MR. MATHEWS:</p> <p>21 Q Is the source pad made of the same piece</p> <p>22 of first conductive layer as the gate pad and the</p> | <p style="text-align: right;">Page 21</p> <p>1 Q And --</p> <p>2 A First conductive layers.</p> <p>3 Q Separate first conductive layer --</p> <p>4 A Right.</p> <p>5 Q -- structures?</p> <p>6 A Right.</p> <p>7 Q In claim 10 and 11 -- let's focus on one</p> <p>8 of those first conductive layer structures.</p> <p>9 A Uh-huh.</p> <p>10 Q In claims 10 and 11 are the source pad,</p> <p>11 gate electrode and gate pad all made at a</p> <p>12 single source -- what was the phrase -- first</p> <p>13 conductive layer structure?</p> <p>14 MR. GOODWYN: Objection. Compound.</p> <p>15 THE WITNESS: I'm not sure I understand</p> <p>16 what the question is.</p> <p>17 BY MR. MATHEWS:</p> <p>18 Q What don't you understand?</p> <p>19 A I -- I don't understand what you're</p> <p>20 trying to distinguish. Things which are part of</p> <p>21 the same conducting piece or not part of the same</p> <p>22 conducting piece or so on?</p> |

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| <p style="text-align: right;">Page 326</p> <p>1 MR. MATHEWS: Okay.</p> <p>2 MR. GOODWYN: -- on our team as well.</p> <p>3 MR. MATHEWS: Okay. That's fine.</p> <p>4 Anything else?</p> <p>5 MR. GOODWYN: Nothing else.</p> <p>6 MR. MATHEWS: Okay. Oh, I suppose I</p> <p>7 should designate as attorneys' eyes only the entire</p> <p>8 testimony today and the basis for that would be to</p> <p>9 the extent that you have talked about CPT's</p> <p>10 processes or structures or any of those materials</p> <p>11 were used as a -- as exhibits in today's</p> <p>12 deposition, we would ask that all those be treated</p> <p>13 as confidential/attorneys' eyes only under the</p> <p>14 protective order.</p> <p>15 VIDEO TECHNICIAN: Okay. The time is</p> <p>16 5:24:22. We're going off the record. This is the</p> <p>17 end of tape number four and the end of today's</p> <p>18 deposition.</p> <p>19 (Whereupon, at 5:24 p.m., the</p> <p>20 deposition of GARY RUBLOFF, PH.D.</p> <p>21 was concluded.)</p> <p>22 * * * * *</p> | <p style="text-align: right;">Page 328</p> <p>1 Deponent Dr. Gary Rubloff c/o</p> <p>2 Morgan Lewis</p> <p>3 1111 Pennsylvania Avenue, NW</p> <p>4 Washington, DC 20004</p> <p>5 Case: LG Phillips LCD v. Tatung Co of America et al</p> <p>6 Date of deposition: 10/27/2005</p> <p>7 Deponent: Dr. Gary Rubloff</p> <p>8 Please be advised that the transcript in the above</p> <p>9 referenced matter is now complete and ready for signature.</p> <p>10 The deponent may come to this office to sign the transcript,</p> <p>11 a copy may be purchased for the witness to review and sign,</p> <p>12 or the deponent and/or counsel may waive the option of signing.</p> <p>13 Please advise us of the option selected.</p> <p>14</p> <p>15 Please forward the errata sheet and the original signed</p> <p>16 signature page to counsel noticing the deposition, noting the applicable</p> <p>17 time period allowed for such by the governing Rules of Procedure.</p> <p>18 If you have any questions, please do not hesitate to call our office at</p> <p>19 202-232-0646.</p> <p>20 Sincerely,</p> <p>21 Digital Evidence Group</p> <p>22 Copyright 2005 Digital Evidence Group</p> <p>Copying is forbidden, including electronically, absent express written consent.</p> |
| <p style="text-align: right;">Page 327</p> <p>1 CERTIFICATE OF NOTARY PUBLIC</p> <p>2 I, SHARI R. BROUSSARD, the officer before whom</p> <p>3 the foregoing deposition was taken, do hereby</p> <p>4 certify that the witness whose testimony appears in</p> <p>5 the foregoing deposition was duly sworn by me; that</p> <p>6 the testimony of said witness was taken by me in</p> <p>7 stenotypy and thereafter reduced to typewriting</p> <p>8 under my direction; that said deposition is a true</p> <p>9 record of the testimony given by said witness; that</p> <p>10 I am neither counsel for, related to, nor employed</p> <p>11 by and of the parties to the action in which this</p> <p>12 deposition was taken; and, further, that I am not a</p> <p>13 relative or employee of any counsel or attorney</p> <p>14 employed by the parties hereto, nor financially or</p> <p>15 otherwise interested in the outcome of this action.</p> <p>16</p> <p>17</p> <p>18</p> <p>19 SHARI R. BROUSSARD</p> <p>20 Notary Public in and for the</p> <p>21 District of Columbia</p> <p>22 My commission expires:</p> <p>July 14, 2010</p> | <p style="text-align: right;">Page 329</p> <p>1 Digital Evidence Group, L.L.C.</p> <p>2 11 Dupont Circle, Northwest, Suite 400</p> <p>3 Washington, D.C. 20036</p> <p>4 (202) 232-0646</p> <p>5</p> <p style="text-align: center;">SIGNATURE PAGE</p> <p>6</p> <p>7 Case Name: LG Phillips LCD v. Tatung Co of America et al</p> <p>8</p> <p>9 Witness Name: Dr. Gary Rubloff</p> <p>10</p> <p>11 Deposition Date: 10/27/2005</p> <p>12</p> <p>13 I do hereby acknowledge that I have read</p> <p>14 and examined the foregoing pages</p> <p>15 of the transcript of my deposition and that:</p> <p>16</p> <p>17 (Check appropriate box):</p> <p>18 () The same is a true, correct and</p> <p>19 complete transcription of the answers given by</p> <p>20 me to the questions therein recorded.</p> <p>21 () Except for the changes noted in the</p> <p>22 attached Errata Sheet, the same is a true,</p> <p>correct and complete transcription of the</p> <p>answers given by me to the questions therein</p> <p>recorded.</p> <p>DATE _____</p> <p>WITNESS SIGNATURE _____</p> |

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| Page 330 | |
| 1 | Digital Evidence Group, L.L.C. |
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| ERRATA SHEET | |
| 6 | |
| Case Name: LG Phillips LCD v. Tatung Co of America et al | |
| 7 | |
| Witness Name: Dr. Gary Rubloff | |
| 8 | |
| Deposition Date: 10/27/2005 | |
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| Page No. Line No. Change | |
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| 22 | Signature _____ Date _____ |

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EXHIBIT C-12

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

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ATTORNEY DOCKET NO. 04805.0110-01000

Assistant Commissioner
for Patents
Washington, D.C. 20231

U.S. Patent Application

Title: LIQUID CRYSTAL DISPLAY DEVICE AND A METHOD OF
MANUFACTURING THE SAME

Inventor(s): Woo Sup SHIN

Serial No: 08/781,188

Group Art Unit: 2515

Filed: January 10, 1997

Examiner: NGUYEN, T.

Allowed: February 17, 1998

Batch No.: A54

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, applicant respectfully
requests that the documents listed on the attached PTO Form 1449
be placed in the file of the above-identified application.

The attached documents were filed in the U.S. Patent and
Trademark Office on July 2, 1997 in the parent application serial
no. 08/616,291 filed on March 15, 1996.

Applicant has advised the undersigned that, in his opinion,
these documents are not material to patentability of the allowed
claims 7-9, 11, 13-15, and 17-20.

If there is any fee due in connection with the filing of this
Statement, please charge the fee to our Deposit Account No.
06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: 

Ernest F. Chapman
Reg. No. 25,961

Dated: May 15, 1998

OMB No. 0651-0011

| | | |
|---|---|---------------------------------|
| INFORMATION DISCLOSURE CITATION (Use several sheets if necessary) | Atty. Docket No. 04805.0110-01000 | Serial No. 08/781,188 |
| | Applicant Woo Sup SHIN | |
| | Filing Date January 10, 1997 | Group 2515 |

U.S. PATENT DOCUMENTS

| *Examiner Initial | Document Number | Date | Name | Class | Sub Class | Filing Date If Appropriate |
|-------------------|-----------------|---------|--------------|-------|-----------|----------------------------|
| | 5,327,001 | 7/5/94 | Wakai et al. | 257 | 350 | |
| | 5,229,644 | 7/20/93 | Wakai et al. | 257 | 749 | |
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FOREIGN PATENT DOCUMENTS

| | Document Number | Date | Country | Class | Sub Class | Translation | |
|---|-----------------|----------|----------------|-------|-----------|-------------|----|
| | | | | | | Yes | No |
| ✓ | 0 530 834 | 3/10/93 | European | | | | |
| ✓ | 2 253 938 | 9/23/92 | United Kingdom | | | | |
| ✓ | 0 449 123 | 10/2/91 | European | | | | |
| ✓ | 0 622 659 | 11/2/94 | European | | | | |
| ✓ | 0 571 108 | 11/24/93 | European | | | | |
| ✓ | 0 484 965 | 5/13/92 | European | | | | |
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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| Examiner | Date Considered | |

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Joint Exhibit F-1 Excerpts

| | | |
|------------------------------|-------------------------------------|----------------------------------|
| Office Action Summary | Application No. <u>08/918114</u> | Applicant(s) <u>Phu et al</u> |
| | Examiner <u>Ngan Nye</u> | Group Art Unit <u>2814</u> |

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

☐ Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
☐ If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
☐ If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
☐ Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 8-10-97
☐ This action is FINAL.
☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1 to 26 is/are pending in the application.
 Of the above claim(s) 9 to 26 is/are withdrawn from consideration.
☐ Claim(s) _____ is/are allowed.
☒ Claim(s) 1 to 8 is/are rejected.
☐ Claim(s) _____ is/are objected to.
☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been received.
☐ received in Application No. (Series Code/Serial Number) _____
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 *Certified copies not received: _____

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4 ☐ Interview Summary, PTO-413
☒ Notice of References Cited, PTO-892 ☐ Notice of Informal Patent Application, PTO-152
☐ Notice of Draftsperson's Patent Drawing Review, PTO-948 ☐ Other _____

Office Action Summary

U. S. Patent and Trademark Office
PTO-326 (Rev. 3-97)

U.S. GPO: 1997-417-381/62710

Part of Paper No. 7LGD 108733
Del. 06-726. et al.

Serial Number: 08/918,119

Page 2

Art Unit: 2814

The response filed August 10, 1998 has been entered and made of record as paper no. 6.

Applicant's election of claims 1-8 in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al..

Wei discloses in figures 15 a thin-film transistor comprising a substrate(12), a gate having a first metal layer(14) and a second metal layer(16), a first insulating layer(28), a semiconductor layer(30), an ohmic contact layer(32), a source and drain electrodes(36), and a second insulating layer(48). Wei teaches on lines 8 of column 9 "a fraction of a micron to several microns". Therefore, it would have been obvious that 1 to 4 microns claimed by Applicants are within the range taught by Wei.

Claims 3, 4, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al as applied to claims 1, 2, 5, and 6 above, and further in view of Miyago et al(cited by Applicants).

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Page 3

Art Unit: 2814

Miyago teaches the gate including a first layer formed of Al and a second layer formed of Mo. It would have been obvious to one of ordinary skill in the art to use the teachings of Wei and Miyago to form the claimed device.

The other references are cited to show other structures pertinent to Applicants' disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (703) 308-4938. The fax phone number for the Art unit is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.



Ngan Van Ngo
Primary Examiner

Ngan Ngo

August 14, 1998

LGD 108735
Del. 06-726. et al.

Attorney Docket No.: 39611.2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Byung-Chul AHN et al.

Serial No.: 08/918,119

Filed: August 27, 1997

For: THIN FILM TRANSISTOR AND METHOD OF MAKING SAME

Assistant Commissioner for Patents
Washington, D.C. 20231



Date: November 17, 1998

Group Art Unit: 2814

Examiner: N. NGO

AMENDMENT

Sir:

In response to the Office Action issued on August 20, 1998, please consider the above-identified patent application amended as follows:

IN THE CLAIMS:

RECEIVED
NOV 25 1998
GROUP 2100

Please amend the claims as follows:

1. (Amended) A thin film transistor comprising:

a substrate; and

a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the [substrate] first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm .

511/58434.01
11/798/1355/39611.00002

LGD 108797
Del. 06-726. et al.

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8. (Amended) A thin film transistor comprising:

a substrate;

A2 a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the [substrate] first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm ;

a first insulating layer disposed on the substrate including the gate;

a semiconductor layer disposed on a portion of the first insulating layer at a location corresponding to the gate;

an ohmic contact layer disposed on two sides of the semiconductor layer;

a source electrode and a drain electrode disposed on the ohmic contact layer and extending onto the first insulating layer; and

a second insulating layer covering the semiconductor layer, the source and drain electrodes and the first insulating layer.

Please cancel claims 3, 7 and 9-26 without prejudice or disclaimer of the subject matter recited therein.

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111798/1355/39611.00002

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LGD 108798
Del. 06-726. et al.

REMARKS

Claims 1-9 are pending in this application. By this amendment, Applicant amends claims 1 and 5 and cancels claims 3, 7 and 9-26.

Claims 1, 2, 5 and 6 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Wei et al. (U.S. Patent No. 5,156,986). Claims 3, 4, 7 and 8 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Wei in view of Miyago et al. (U.S. Patent No. 5,036,370).

Applicant has amended claims 1 and 5 to recite:

"a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm "

As described in the present specification, Applicant's claimed invention provides a solution to a problem which occurs when Aluminum is used as a bottom layer for a double-layered gate. This problem is that hillock occurs at the sides of the Aluminum bottom layer and causes improper functioning of the TFT. Applicant's claimed combinations including the gate structure noted above eliminates hillock at the sides of the Aluminum bottom layer of the gate by arranging the second metal layer to prevent hillock and to be smaller than the first metal layer (Al layer) by about 1 to 4 μm .

In contrast, Wei teaches a gate having a double-layered structure in which the bottom layers are either Ti or Chromium, which do not experience hillock. In addition, Wei did not even recognize any hillock problems or solutions thereto because Wei does not use an aluminum layer to form a gate.

Miyago does use an aluminum layer in a double-layered gate and does recognize a hillock problem which occurs along a top surface of a bottom aluminum layer located between the aluminum layer and a top layer. Miyago provides an entirely different solution by providing a clad structure for causing the top-surface hillock

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Del. 06-726. et al.

problem to be reduced. More specifically, Miyago teaches that in order to solve the top-surface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure and then a TaOx layer is put on the Ta layer. Miyago fails to recognize the side hillock problem with the aluminum bottom layer and also fails to recognize the necessity or desirability for Applicant's claimed second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer and the first metal layer being wider than the second metal layer by about 1 to 4 μm .

In view of the foregoing remarks, Applicant respectfully submits that claims 1 and 5 are allowable. Claims 2, 4 and 6, 8 and 9 are dependent upon claims 1 and 5, respectively, and are therefore allowable for at least the reasons that claims 1 and 5 are allowable.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service to Addressee as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on November 17, 1998:

Respectfully submitted,

Joseph R. Keating

Name of Registered Representative

[Signature]
Signature

November 17, 1998
Date of Signature

[Signature]
Joseph R. Keating
Registration No. 37,363
Graham & James, LLP
885 Third Avenue, 21st Floor
New York, New York 10022
Telephone: (212) 648-1600

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TOTAL PAGES

LGD 108800
Del. 06-726. et al.

EXHIBIT FGH-2

US005156986A

United States Patent [19][11] **Patent Number:** **5,156,986****Wei et al.**[45] **Date of Patent:** **Oct. 20, 1992**

[54] **POSITIVE CONTROL OF THE SOURCE/DRAIN-GATE OVERLAP IN SELF-ALIGNED TFTS VIA A TOP HAT GATE ELECTRODE CONFIGURATION**

0173340 7/1988 Japan 437/44
 0120068 5/1989 Japan 357/23.7
 0133371 5/1989 Japan 437/44
 0209764 8/1989 Japan 357/23.7

[75] **Inventors:** **Ching-Yeu Wei; George E. Possin; Robert F. Kwasnick**, all of Schenectady, N.Y.

[73] **Assignee:** **General Electric Company**, Schenectady, N.Y.

[21] **Appl. No.:** **667,149**

[22] **Filed:** **Mar. 11, 1991**

Related U.S. Application Data

[62] Division of Ser. No. 593,423, Oct. 5, 1990, abandoned.

[51] **Int. Cl.⁵** **H01L 21/336; H01L 21/28**

[52] **U.S. Cl.** **437/40; 437/44; 437/101; 437/909; 357/23.7**

[58] **Field of Search** **437/40, 41, 44, 101, 437/245, 246, 228, 909; 156/649, 656, 667; 357/4, 23.7, 2**

[56] References Cited**U.S. PATENT DOCUMENTS**

4,651,185 3/1987 Holmberg et al. 357/23.7
 4,700,458 10/1987 Suzuki et al. 437/83
 4,767,723 8/1988 Hinsberg, III et al. 437/41
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 4,963,504 10/1990 Huang 437/233
 4,978,626 12/1990 Poon et al. 437/233
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 5,015,599 5/1991 Verhaar 437/233
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 5,036,370 7/1991 Miyago et al. 357/4
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OTHER PUBLICATIONS

Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1 *Process Technology*, Lattice Press 1986, p. 558.

T. Kodama et al., A Self-Alignment Process for Amorphous Silicon Thin Film Transistors, *IEEE Electron Device Letters*, vol. EDL-3, No. 7, Jul. 1982.

K. Asama et al., A Self-Alignment Process a-Si TFT Matrix Circuit for LCD Panels, Fujitsu, Laboratories, Ltd., Atsugi, Japan, *SID Digest*, 1983.

S. Nisha et al., A New Self-Aligned A-Si TFT Using Ion Doping and Chromium Silicide Formation, #A6.1, *Symposia Abstracts for Materials Research Society*, 1991, Spring Meeting, p. 32.

Primary Examiner—Mary Wilczewski

Attorney, Agent, or Firm—Donald S. Ingraham; James C. Davis, Jr.; Marvin Snyder

[57] ABSTRACT

Positive control over the length of the overlap between the gate electrode and the source and drain electrodes in a thin film transistor is provided by a gate conductor layer comprising two different conductors having differing etching characteristics. As part of the gate conductor pattern definition process, both gate conductors are etched to expose the underlying material and the upper gate conductor layer is etched back to expose the first gate conductor layer in accordance with the desired overlap between the gate electrode and the source and drain electrodes. Thereafter, the remainder of the device is fabricated with the source and drain electrodes self-aligned with respect to the second gate conductor layer using a planarization and non-selective etch method.

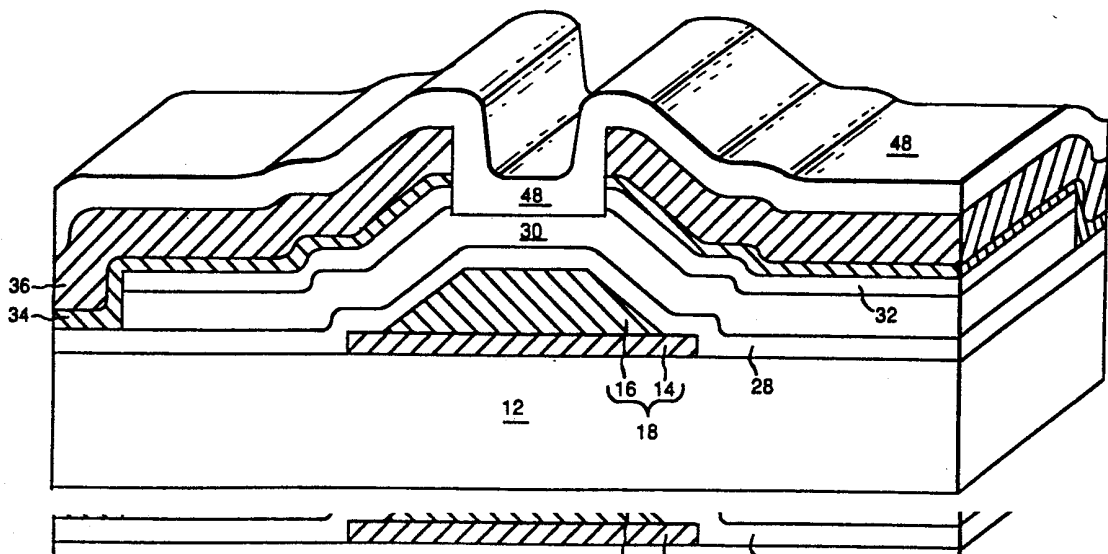
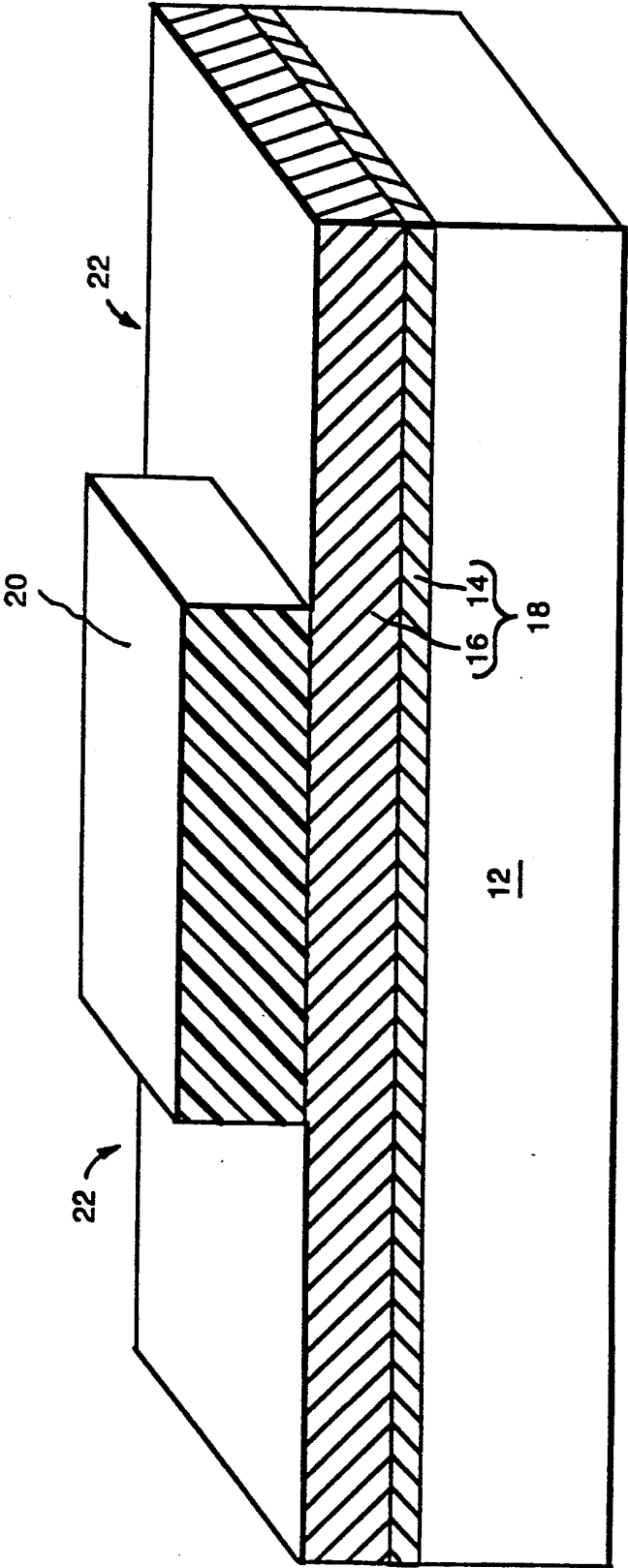
13 Claims, 15 Drawing Sheets

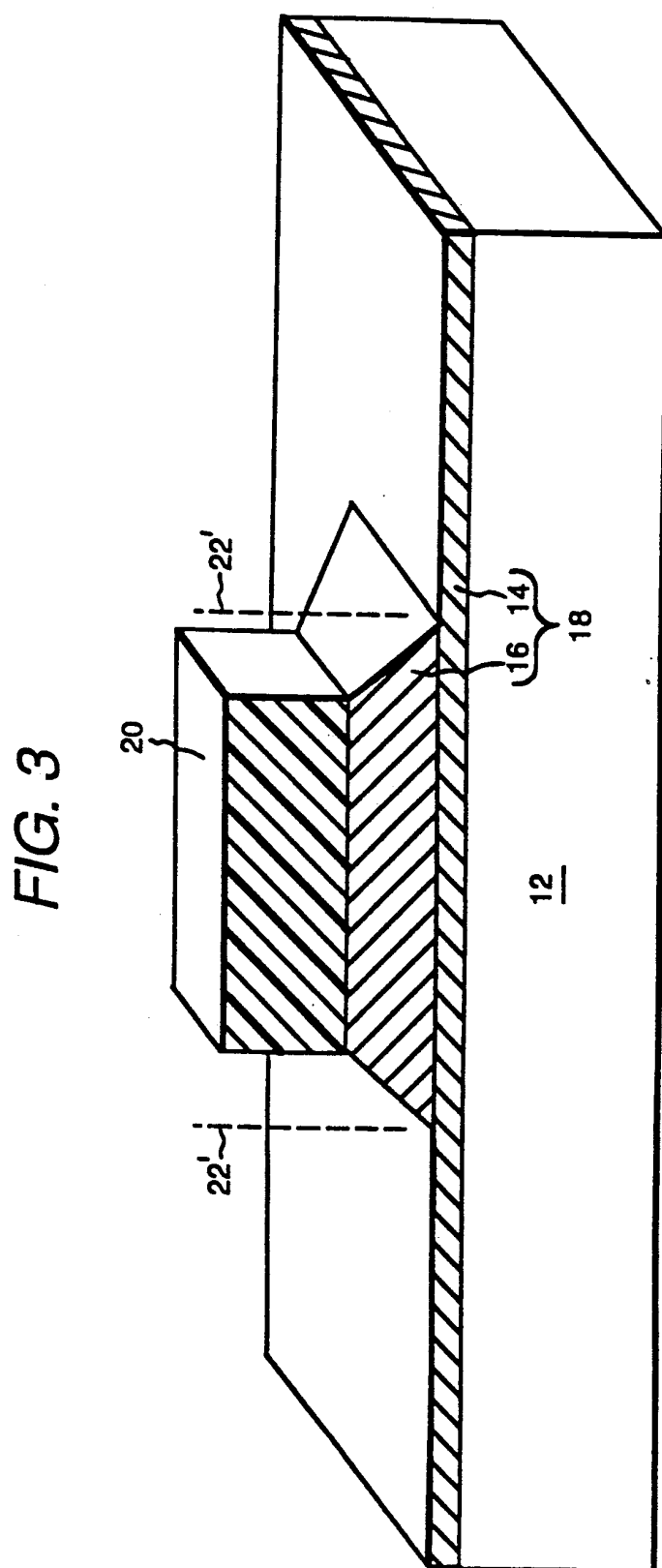
FIG. 1

16 14 }
18

12

FIG. 2





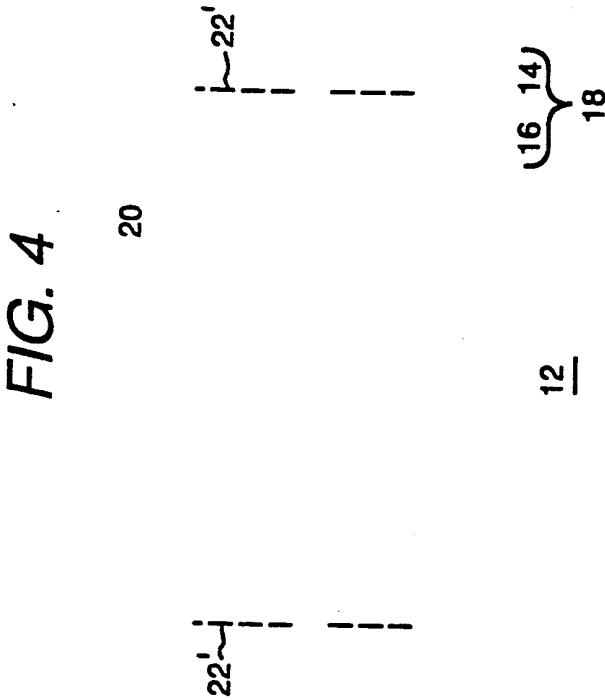


FIG. 5

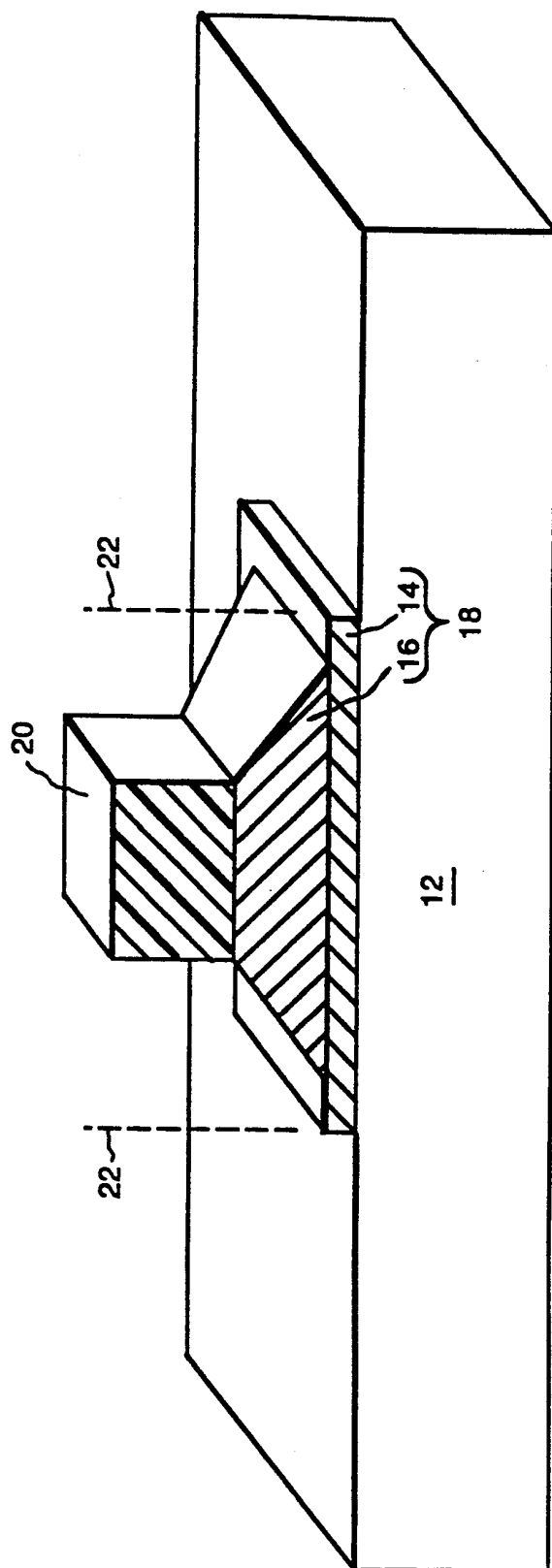
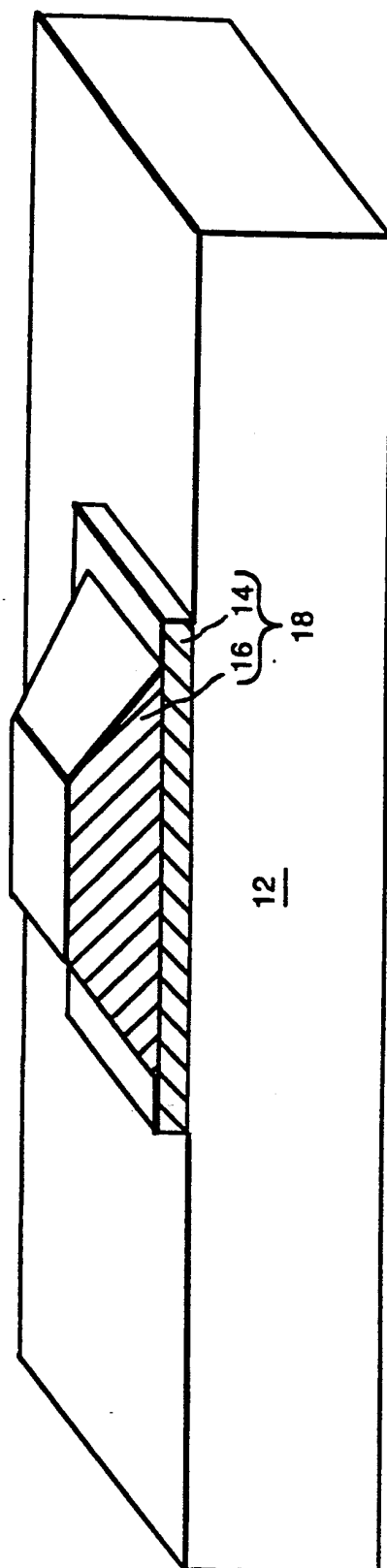


FIG. 6



U.S. Patent

Oct. 20, 1992

Sheet 7 of 15

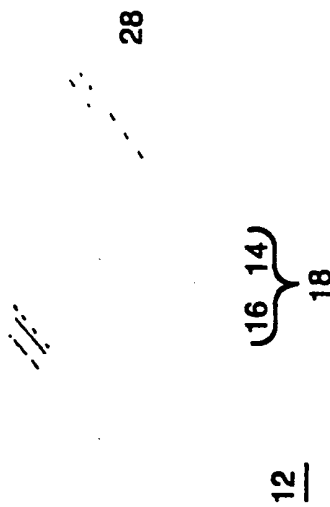
5,156,986**FIG. 7**

FIG. 8

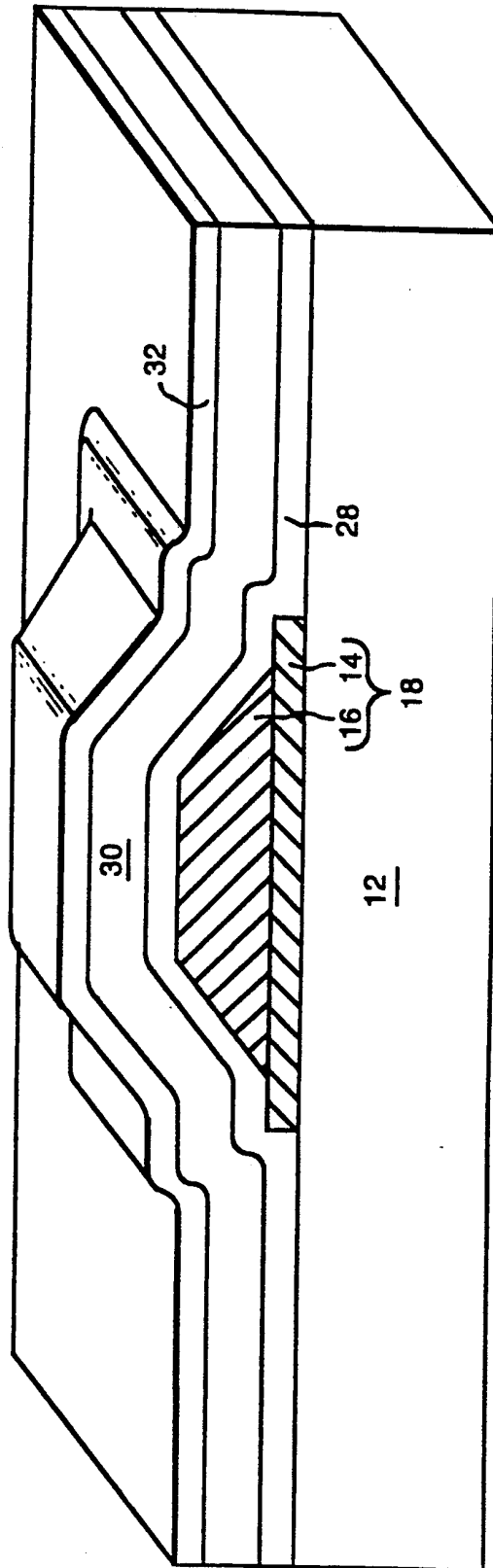


FIG. 9

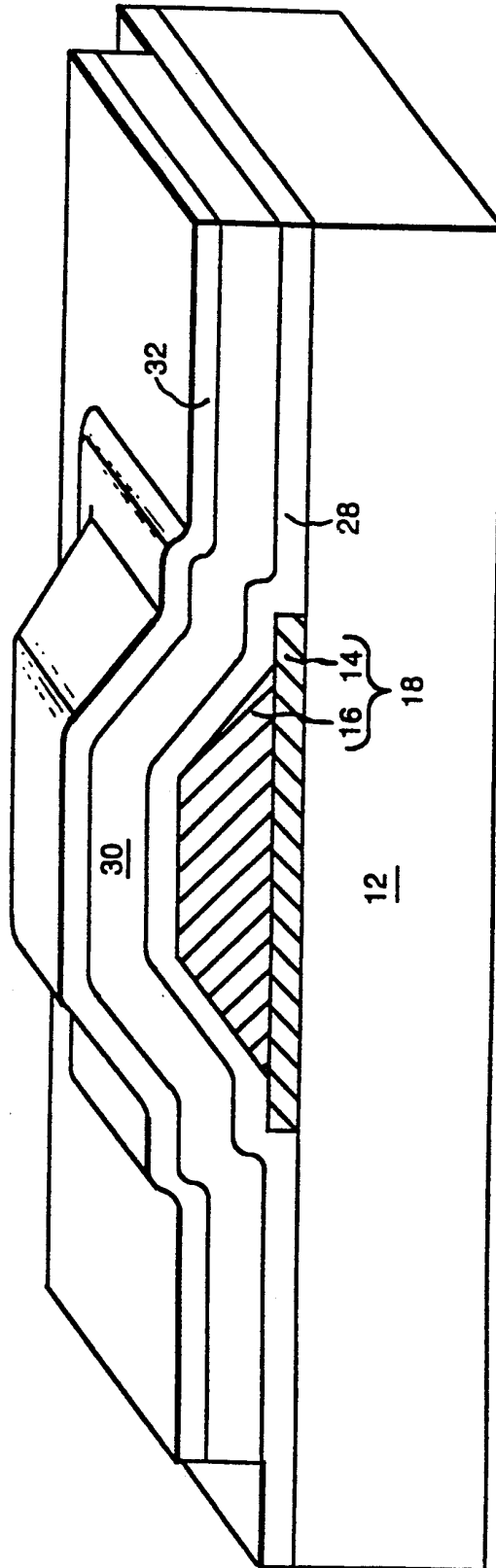


FIG. 10

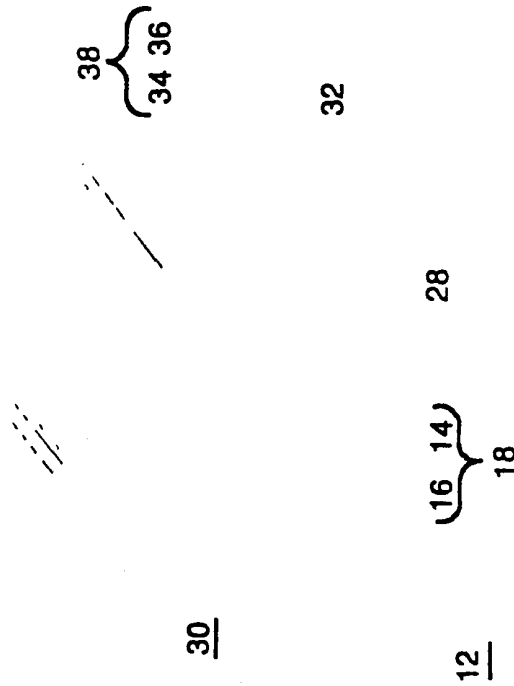


FIG. 11

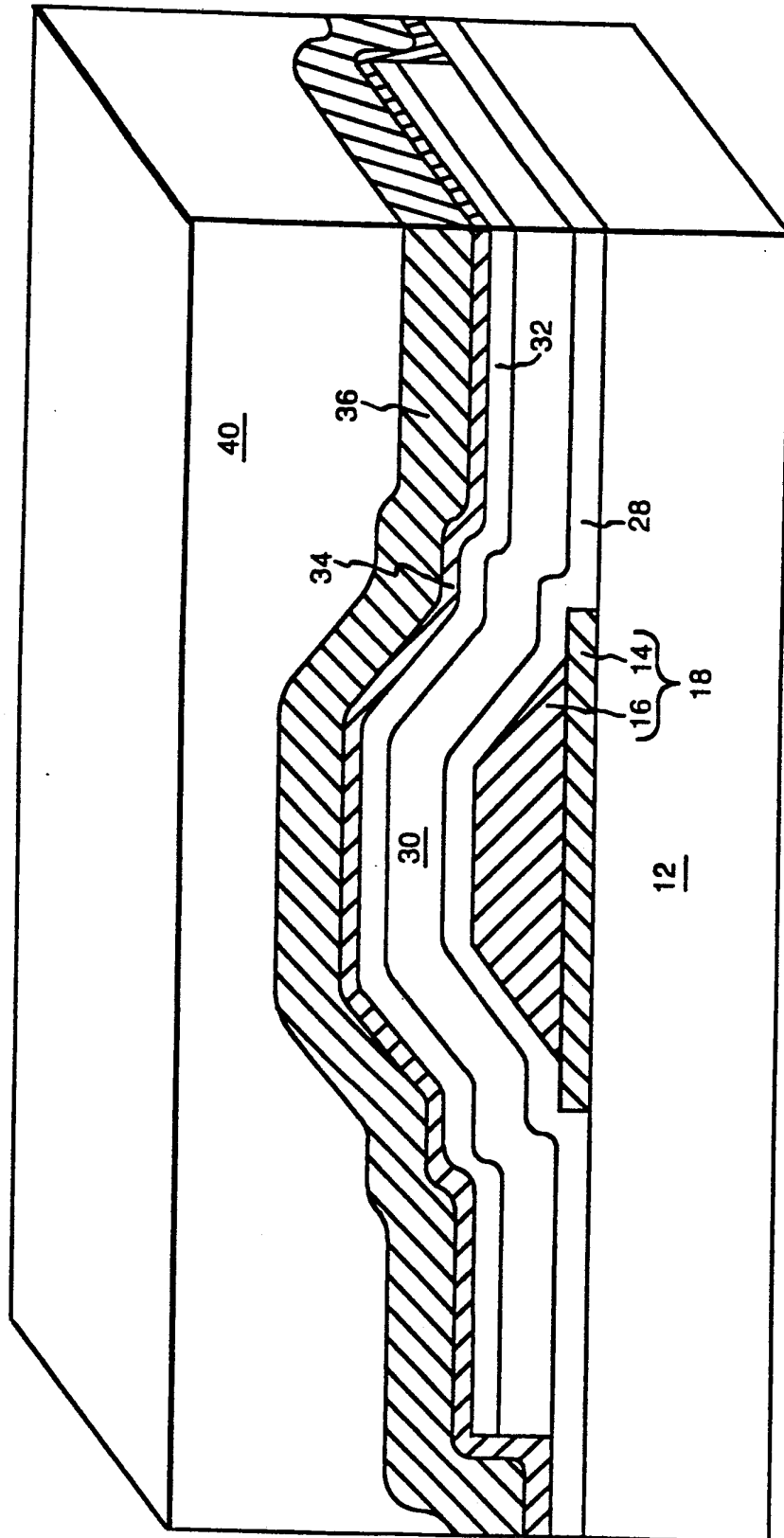


FIG. 12

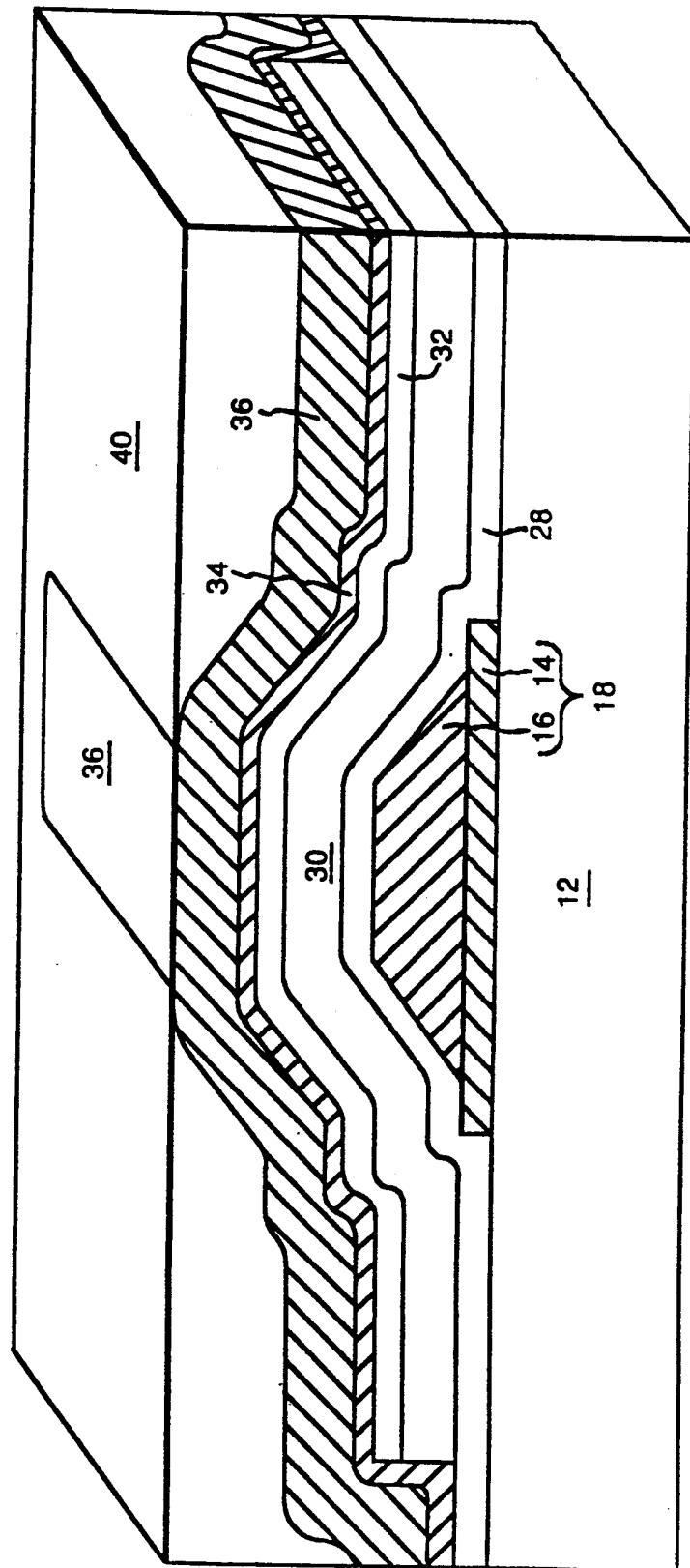


FIG. 13

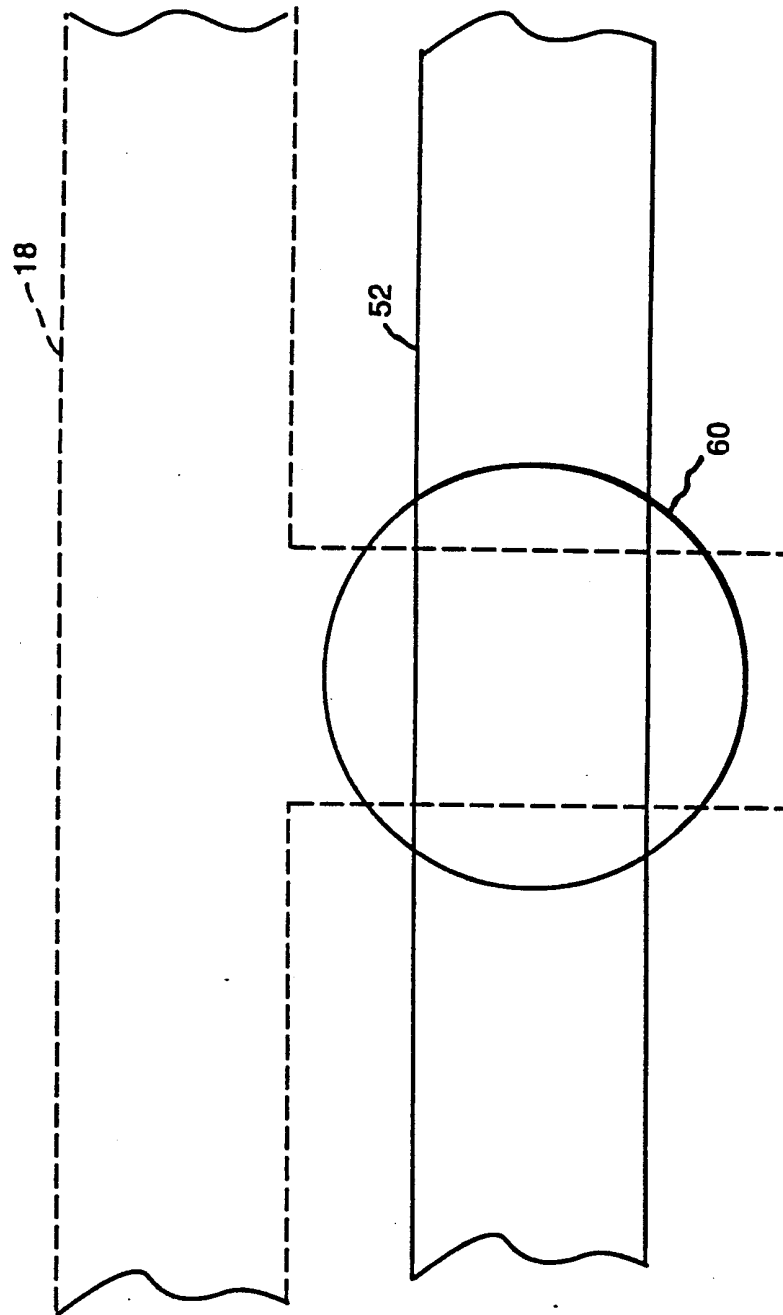


FIG. 14

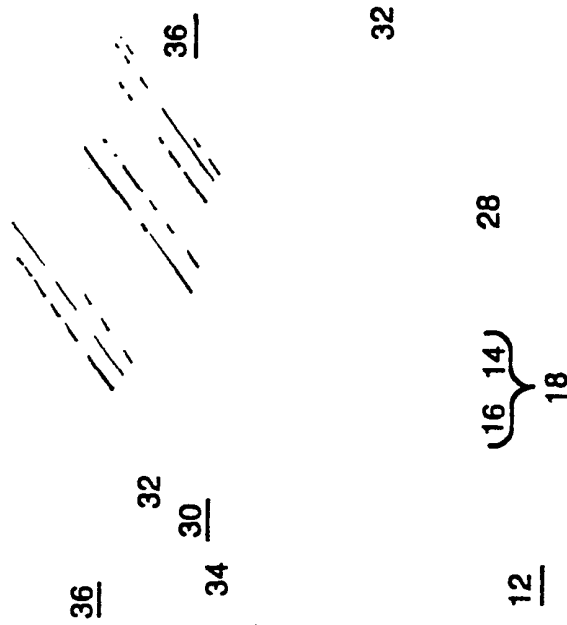
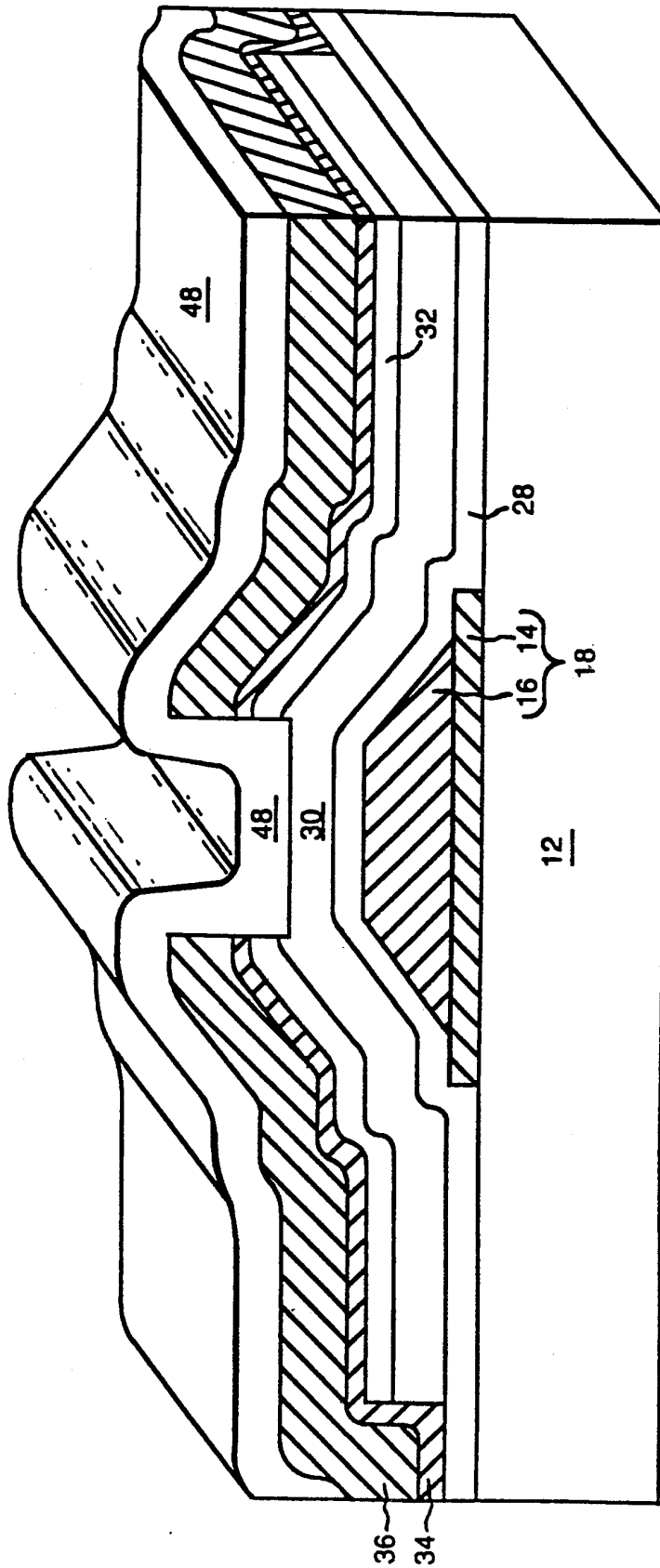


FIG. 15



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POSITIVE CONTROL OF THE SOURCE/DRAIN-GATE OVERLAP IN SELF-ALIGNED TFTS VIA A TOP HAT GATE ELECTRODE CONFIGURATION

This application is a division of application Ser. No. 07/593,423, filed Oct. 5, 1990, now abandoned.

RELATED APPLICATIONS

The present application is related to application Ser. No. 07/593,419, filed Oct. 5, 1990, entitled, "Thin Film Transistor Structure With Improved Source/Drain Contacts", by R. F. Kwasnick, et al.; application Ser. No. 07/593,425, filed Oct. 5, 1990, entitled "Device Self-Alignment by Propagation of a Reference Structure's Topography", by C-Y Wei, et al.; application Ser. No. 07/593,421, filed Oct. 5, 1990, entitled, "Thin Film Transistor Having an Improved Gate Structure and Gate Coverage by the Gate Dielectric" by R. F. Kwasnick, et al.; application Ser. No. 07/510,767, filed Apr. 17, 1990, entitled "Method for Photolithographically Forming a Self-Aligned Mask Using Back Side Exposure and a Non-Specular Reflecting Layer", by G. E. Possin, et al.; and application Ser. No. 07/499,733, filed Mar. 21, 1990, entitled "Method for Fabricating a Self-Aligned Thin-Film Transistor Utilizing Planarization and Back-Side Photoresist Exposure", by G. E. Possin, et al., now U.S. Pat. No. 5,010,027, each of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the field of fabrication techniques for thin film transistors, and more particularly to techniques for self-aligned fabrication of thin film transistors.

Background Information

Thin film transistors (TFTs) are employed in liquid crystal displays and imagers to control or sense the state of each pixel of the display or image. At present, such thin film transistors are typically fabricated from amorphous silicon. In such display or sensor systems, system operating characteristics are optimized by making each cell or pixel have substantially identical operating characteristics. These operating characteristics include switching speed, capacitive loading of drive and sense lines, the gain of transistors and so forth.

One of the processing problems which causes variation in the characteristics of different cells within such structures is the inability to accurately align the position of a mask which defines the source and drain electrodes of thin film transistors in a manner which ensures that the source/drain electrodes are accurately aligned with respect to the gate electrodes. Misalignment results in an increase in the overlap between the gate electrode and either the source electrode or the drain electrode with a corresponding decrease in the overlap between the gate and the other of them. Since the capacitances between the gate electrode and the source or drain electrodes are direct functions of the overlap between them, such a change in overlap produces a change in device's capacitances and consequently, switching speed and loading of other circuits. The possibility of misalignment requires that the size of the gate metal be increased to ensure that all devices have acceptable overlap between the gate and the source and drain. This

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increases the device size and hence the total capacitance per device. The device capacitance is important because it controls the charging time of the gate electrodes, the capacitive coupling between the gate and the source and drain nodes, and the noise introduced by the defects in the amorphous silicon or at the amorphous silicon/dielectric interface. Consequently, there is a desire to provide self-alignment between the source and drain electrodes and the gate electrode in order to maintain a fixed, predictable overlap between the gate electrode and each of the source and drain electrodes across an entire wafer.

A variety of self-alignment techniques have been proposed or developed. The above-identified related applications Ser. Nos. 07/499,733 and 07/510,767 each disclose techniques for obtaining self-alignment between the gate electrode and the source and drain electrodes through the use of through-the-substrate exposure of photoresist. Such processes result in specific gate-to-source and gate-to-drain overlaps which are peculiar to those techniques and the particular manner in which they are carried out. Those overlaps may be smaller or larger than optimum. Such a through-the-substrate exposure technique is not suitable where the semiconductor itself or another device layer would absorb the light needed to expose the photoresist. Consequently, there is a need for other self-alignment techniques for thin film transistors.

Related application Ser. No. 07/593,425 solves these problems by employing mechanical propagation of topographical features of a lower, reference layer, upward through subsequently deposited layers of the structure, including a support layer. A subordinate layer (source/drain metallization) is deposited on the support layer and may be either conformal or not conformal. If necessary, a planarization layer is formed over the subordinate layer to provide a planar upper surface for the structure. Material is then removed from the upper surface in a non-selective, uniform manner until the source/drain metallization becomes exposed in an aperture which is thereby created in the planarization layer in alignment with the underlying reference layer pattern. The exposed portion of the subordinate layer is then selectively etched to expose the support layer. Alternatively, the planarization etch could be continued until the support layer was exposed, but that would result in thinner source and drain electrodes. Other portions of the subordinate layer are then patterned, if necessary and the fabrication of the device completed. The result is a device in which the overlap of the subordinate layer over the reference pattern in the vicinity of the aperture in the subordinate layer is self-aligned with respect to the reference layer pattern.

The technique of application Ser. No. 07/593,425 can provide a very short overlap between the gate electrode and the source and drain electrodes. In particular, an overlap of less than 0.5 μm is achievable. Such a small overlap is desirable from the point of view of minimizing overlap capacitance and capacitance induced noise. Unfortunately, it is found experimentally that there is a minimum overlap between the gate and the source and drain electrodes below which the saturation drain current of a TFT degrades significantly. While the minimum length of this overlap for good device operating characteristics may vary with different semiconductor materials and other variations in the device structure, it would be desirable to have a technique for positively

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controlling the amount of overlap between the gate electrode and the source and drain electrodes in a self-aligned TFT structure.

OBJECTS OF THE INVENTION

Accordingly, a primary object of the present invention is to provide a technique for positively controlling the length of the overlap between the gate electrode and the source and drain electrodes in a self-aligned thin film transistor.

Another object of the present invention is to increase the versatility of the self-alignment technique disclosed in related application Ser. No. 07/593,425.

Another object of the present invention is to provide a self-alignment method which is applicable to opaque substrates.

SUMMARY OF THE INVENTION

The above and other objects which will become apparent from the specification as a whole, including the drawings, are accomplished in accordance with the present invention by fabricating the gate electrode as two separate layers of different conductors; patterning the entire gate electrode to the desired gate electrode pattern and subsequently etching the second layer of the gate electrode conductor back from the edges of the first level gate electrode conductor in a self-aligned manner whereby positive control of the degree of setback of the tapered edge of the upper layer (thick) gate conductor material from the lower layer (thin) conductor material is provided while retaining self-alignment. In this manner, a self-aligned process which relies on propagation of the topography of the gate electrode through subsequently deposited layers of the structure provides gate-to-source and gate-to-drain electrode overlaps which are controlled by the setback of the second gate conductor layer with respect to the first gate conductor layer in addition to the setback produced by the slope of the tapered second gate conductor layer.

In accordance with one embodiment of the invention, the first and second gate conductor layers are sequentially deposited on a substrate in the same vacuum pumpdown, the gate conductor is photomasked and etched to expose the substrate in the areas where the gate conductor is not desired. Thereafter, the second gate conductor layer is etched back from the edge of the first conductor layer using the same gate mask and an etchant to which the first gate conductor layer is substantially immune and with a technique which tapers the second gate conductor layer to provide lateral edges on that layer which are suitable for the deposition of conformal layers thereover. Thereafter, substantially conformal gate dielectric and semiconductor layers are deposited on the structure followed by patterning of the semiconductor layers and then deposition of source/-drain metallization which may be conformal or nonconformal. Where the source/drain metallization does not exhibit a planar upper surface, a planarization layer is deposited on top of the source/drain metallization to provide a planar upper surface for the device structure. The device structure is then etched in a non-selective manner until the source/drain metallization is exposed in alignment with the raised (thick) portion of the gate electrode pattern. The exposed portion of the source/-drain metallization is then selectively etched to expose the n⁺ amorphous silicon which is then removed. Thereafter, back channel passivation may be provided

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on the upper surface of the structure to minimize the effect of external conditions on the operating characteristics of the device.

The resulting semiconductor device has a setback or top hat gate conductor configuration in which the effective electrical gate width is that of the thin, lower, wider gate conductor layer while the configuration of the thicker, upper, narrower gate conductor layer controls the self-alignment of the source and drain electrodes with respect to the gate electrode and thus the overlap between the source and drain electrodes and the gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of practice, together with further objects and advantages thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings in which:

FIGS. 1-14 illustrate successive stages in the fabrication of a thin film transistor in accordance with the present invention;

FIG. 1 is a perspective, partially cross section view of a substrate having an unpatterned reference layer disposed thereon;

FIG. 2 is a perspective, partially cross section view of the FIG. 1 structure having a patterned layer of photoresist disposed thereon;

FIG. 3 is a perspective, partially cross section view of the FIG. 2 structure following etching of an upper gate conductor layer;

FIG. 4 is a perspective, partially cross section view of the FIG. 3 structure following etching of a lower gate conductor layer;

FIG. 5 is a perspective, partially cross section view of the structure following etch back of the upper layer of the gate conductor from the edge of the lower gate conductor;

FIG. 6 is a perspective, partially cross-section view of the FIG. 5 structure following stripping of the retained photoresist;

FIG. 7 is a perspective, partially cross-section view of the FIG. 6 structure following the deposition of a gate insulator thereover;

FIG. 8 is a perspective, partially cross-section view of the structure following the deposition of two layers of semiconductor material;

FIG. 9 is a perspective, partially cross-section view of the FIG. 8 structure after patterning of the layers of semiconductor material;

FIG. 10 is a perspective, partially cross-section view of the structure following the deposition of two layers of source/drain metallization;

FIG. 11 is a perspective, partially cross-section view of the structure following completion of the structure through the formation of a substantially planar surface;

FIG. 12 is a plan view of a portion of the structure;

FIG. 13 is a perspective, partially cross-section view of the structure following uniform removal of enough material from the structure to expose the support layer within an aperture in the subordinate layer;

FIG. 14 is a perspective, partially cross-section view of the FIG. 13 structure following etching of the support layer in the self-aligned openings in the subordinate layer; and

FIG. 15 is a perspective, partially cross-section view of the structure following formation of a passivation layer over the structure.

DETAILED DESCRIPTION

In accordance with one embodiment of the present invention, an amorphous silicon thin film (TFT) field effect transistor (FET) may be fabricated. Various stages in the fabrication of such a device in accordance with the present invention are illustrated in FIGS. 1-14.

In FIG. 1, a substrate 12 has a uniform reference layer 18 disposed thereon. Reference layer 18 comprises first and second sublayers 14 and 16. For fabrication of a thin film transistor, the layer 18 constitutes the gate conductor while the substrate 12 constitutes a larger structure on which the transistor is to be disposed. In many applications such as liquid crystal displays and imagers, it is desirable that the substrate 12 be transparent, however, transparency of the substrate is unimportant to the present process and thus, is a matter of design choice in accordance with the intended use of the thin film transistor to be fabricated. Typical transparent substrate materials are glass, quartz and appropriate plastics.

The gate conductor sublayers 14 and 16 are deposited on the substrate in sequence by any appropriate technique such as sputtering, chemical vapor deposition, thermal evaporation and so forth. This gate conductor is comprised of two layers of different metals such as a first layer of titanium disposed in contact with the substrate with a layer of molybdenum or aluminum (referred to as Mo/Ti and Al/Ti metallization, respectively) disposed thereover or a layer of chromium disposed on a substrate with a layer of molybdenum disposed thereover (Mo/Cr metallization). As a further alternative, the first sublayer of the gate conductor may be a transparent conductor material such as indium tin oxide or other transparent conductors. We prefer to use Mo/Cr.

The gate electrode is typically deposited to a thickness of 1,000 Å to 10,000 Å, depending on the sheet resistivity required for the gate electrode structure and the vertical height of the top hat gate required to achieve good self-alignment. With a Mo/Cr gate conductor, the Cr is preferably 100 to 500 Å thick and the Mo is preferably 1000 to 10,000 Å thick.

The FIG. 1 structure is then photomasked to provide a mask pattern corresponding to the desired gate conductor configuration as shown in FIG. 2. The upper surface of the second conductor 16 is exposed in the window 22 where the photoresist 20 has not been retained. Next, the structure is dry etched preferably using reactive ion etching to pattern the upper conductor layer 16 in accordance with the retained photoresist pattern. To do this, the wafer is mounted in a reactive ion etching apparatus which is then purged and evacuated in accordance with normal reactive ion etching procedures. A source gas flow preferably of 37.5 sccm (standard cubic centimeters per minute) of sulphur hexafluoride (SF₆), 6.5 sccm of Cl₂ and 16 sccm of O₂ is established, introduced into the etching chamber at a pressure of 65 mtorr and reactive ion etching potentials are applied to etch the molybdenum in the windows 22. This etching is preferably carried out until all the molybdenum is removed in center of the windows and is allowed to proceed for 40 seconds more of overetching to ensure that all of the molybdenum is removed from within the originally defined windows 22. This molyb-

denum etching step is preferably carried out at a power of 200 watts.

Following this etching step, the structure appears as illustrated in FIG. 3. It will be noted, that the second conductor (molybdenum) has been removed from the structure everywhere outside the region which was initially protected by the retained portion of the photoresist 20. The original edges of the retained photoresist are indicated by the dash lines marked 22', but the photoresist has been etched back from that original edge as the etching of the molybdenum has proceeded. This results in the substantially 45° slope to the side walls of the molybdenum as illustrated in FIG. 3.

A tapered gate electrode of this type may be provided in a variety of other ways well known in the art including reliance on the erosion of the photoresist during etching of the gate conductor where reactive ion etching (RIE) is employed or an isotropic wet etch may be employed which undercuts the resist during etching of the unprotected portion of the gate conductor.

Such a slope is provided in RIE, in part because when the photoresist is baked after patterning to toughen it prior to RIE etching, the photoresist slumps with the result that its thickness tapers from small or zero at the edge of a photoresist region upward to the central thickness of the photoresist over a finite distance. During reactive ion etching, the photoresist erodes as the gate conductor is etched with the result that a taper is produced on the retained portion of the gate conductor.

Next, the etching gas is preferably changed to 70 sccm of Cl₂ and 30 sccm of O₂ at a pressure of 100 mtorr to remove the exposed chromium. This etch is preferably continued until all the exposed chromium appears to have been removed and is then continued for an additional 60 seconds to ensure complete removal of the exposed chromium. The degree of overetching which should be employed depends on the substrate composition and the relative etch rates of the first conductor 14 and the substrate in the etching composition employed. This etching step is preferably carried out at a power of 300 watts. Following this step, the structure appears as illustrated in FIG. 4.

Next, the molybdenum upper layer of the gate conductor is etched back to expose a desired width of the first gate conductor layer. This may be done with the RIE using the same source gases as for the initial etching of the molybdenum, provided that that etchant does not excessively etch the now exposed portion of the substrate where the chromium has been removed. Following this step, the structure appears as illustrated in FIG. 5.

The retained photoresist is then removed to leave the structure illustrated in FIG. 6.

Next, a gate dielectric layer 28 is deposited over the entire structure preferably by chemical vapor deposition or some other process which is known to produce a high integrity dielectric. This gate dielectric is preferably be silicon nitride but may be silicon dioxide or other dielectrics and is about 1,000 to 4000 Å thick. The chromium gate conductor layer 14 is sufficiently thin (10 to 1000 Å) and the sidewall of the molybdenum gate conductor layer 16 is sufficiently vertically inwardly tapered or sloped that a high integrity conformal dielectric layer results.

This deposition of gate dielectric on the upper surface of the structure is done in a conformal manner whereby the raised configuration of the patterned gate electrode extends to the upper surface of that gate dielectric layer,

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that is, the surface topography is essentially unchanged as shown in FIG. 7.

Thereafter, in the fabrication of a typical silicon thin film transistor, a layer 30 of intrinsic amorphous silicon is deposited on the gate dielectric layer in a conformal manner. This intrinsic amorphous silicon layer typically has a thickness on the order of 2,000 Å. A thinner layer 32 (about 500 Å) of doped (typically phosphorous doped, that is n+) amorphous silicon is then deposited on the intrinsic amorphous silicon in a conformal manner to provide the structure illustrated in FIG. 8.

The dielectric layer, the intrinsic amorphous silicon and the doped amorphous silicon may all be deposited in the same deposition chamber without breaking the vacuum. Where that is done, we prefer to stop the plasma discharge in the deposition chamber after the completion of the deposition of a particular layer until after the proper gas composition for the deposition the next layer has been established. We then re-establish the plasma discharge to deposit that new layer. Alternatively, the two silicon depositions may be done in different chambers.

At this stage, the silicon layers may be patterned photolithographically to restrict them to the part of the structure where the silicon is needed, as shown in FIG. 9.

Thereafter, the source/drain metallization is deposited over the structure in a conformal manner. In accordance with application Ser. No. 07/593,419, entitled, "Thin Film Transistor Structure With Improved Source/Drain Contacts", this source/drain metallization is preferably a two layer molybdenum on chromium (Mo/Cr) metallization in which the Cr is 100 to 1000 Å thick and the molybdenum is 1000 to 10,000 Å thick, as shown in FIG. 10. Alternatively, this metallization may be a single metal such as molybdenum, chromium or tungsten. Following this step, the structure appears as illustrated in FIG. 10.

A planarization layer 40 (which may be photoresist) is then formed over the entire structure to provide a substantially planar upper surface of the structure as shown in FIG. 11.

In this manner, the topology of the patterned gate conductor is propagated upward through the various layers, at least through the support layer (the n+ doped amorphous silicon in this example) on which the source/drain metallization is disposed. That propagation of topography could be terminated by the source/drain metallization itself, but is at this time preferably terminated by a separate planarization layer because common metallization deposition processes are substantially conformal in nature and making the source/drain metallization conformal enables the final source and drain electrodes to be thicker.

The entire structure is then etched back in a non-selective manner by a planarization reactive ion etch. This planarization etch is preferably stopped once the molybdenum over the gate electrode has been exposed. That exposed molybdenum is then selectively etched with the remaining portion of the planarization layer serving as the etching mask to restrict that etching to the molybdenum which is over the gate electrode. This is followed by etching the now exposed chromium. As illustrated in FIG. 12, a self-aligned overlap between the source and drain electrodes and the gate electrode is produced. Alternatively, the planarization etch may be continued until the chromium layer of the source/drain metallization has been exposed. That exposed chro-

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mium 34 is then selectively etched to expose the doped silicon 32. As a still further alternative, the planarization etch can be continued until the doped silicon becomes exposed.

At this stage, the exposed doped silicon is removed by etching to leave only intrinsic silicon between the source and drain electrodes. This normally involves the removal of some, but not all of the intrinsic amorphous silicon in order to ensure that all of the doped amorphous silicon has been removed.

A key consideration is that the source/drain gap in the circle 60 in the top down view in FIG. 13 is disposed in proper alignment with the underlying gate electrode 18. Since the source/drain gap is defined by the self-aligned planarization method just described, control of the size of the source/drain gap and its location is independent of the alignment of the etching mask 52 which controls the pattern and location of the other portions of the boundary of the retained source/drain metallization.

If the silicon was not patterned previously it is usually necessary to remove excess silicon exposed after the removal of the source/drain metal. This etch is done with the source/drain mask still in place in order to protect the exposed silicon in the channel region.

The source and drain metallization is then patterned to provide the various desired segments of the source and drain metallization which connect to various devices and interconnect devices in a manner which is appropriate to the structure being fabricated. The etching of the pattern of the source/drain metallization may preferably be done in two stages using RIE with the appropriate source gases discussed above or it may be done by wet etching or other means. This yields the structure illustrated in FIG. 14.

Thereafter, a passivation layer 48 may be deposited on the upper surface of the structure as shown in FIG. 15. This passivation layer is known as a back channel passivation layer since its purpose is to passivate the back or the away-from-the-gate-metallization surface of the silicon to maximize the stability of the device characteristics of this thin film transistor. This passivation layer is typically about 2,000 Å thick and may be silicon dioxide, silicon nitride or other insulators such as polyimide.

Typically, the illustrated thin film transistor is only one of many such thin film transistors which are simultaneously fabricated on the same substrate.

While the semiconductor material in the just described embodiment is amorphous silicon, since that is the material presently in typical use for thin film transistors, it should be understood that this process is equally applicable to the use of other semiconductor materials or other forms of silicon. Further, while the gate dielectric layer has been described as being silicon nitride, it will be understood that more than one sublayer may be present in the gate dielectric layer and various sublayers may have different compositions and a single layer dielectric may be SiO₂ or other dielectric materials.

Other semiconductor materials which are presently used in an amorphous condition are germanium and cadmium selenide. This process technique is applicable to those amorphous silicon semiconductor materials and any others as well as being applicable to polycrystalline or even monocrystalline semiconductor materials where the underlying support structure supports the formation of such semiconductor layers.

It will be recognized that the distance by which the upper gate layer 16 is setback from the edge of the lower gate layer 14 is controlled by the rate at which the upper gate layer etches back and the length of time for which that etch back is allowed to proceed. By appropriate control of the etch rate and time this setback can be varied over a substantial range, from a fraction of a micron to several microns or more as may be considered desirable in a particular device.

This provides the ability to controllably increase the degree of overlap between the gate electrode and the source and drain electrodes of self-aligned device produced in accordance with application Ser. No. 07/593,425, "Device Self-Alignment by Propagation of a Reference Structure's Topography". This technique is also applicable to the methods disclosed in related applications Ser. Nos. application Ser. No. 07/510,767, entitled, "Method for Photolithographically Forming a Self-Aligned Mask Using Back Side Exposure and a Non-Specular Reflecting Layer" and application Ser. No. 07/499,733, entitled, "Method for Fabricating a Self-Aligned Thin-Film Transistor Utilizing Planarization and Back-Side Photoresist Exposure", provided that the first gate metallization layer is made of a material which is transparent or sufficiently transmissive of the actinic light employed to expose the photoresist that the photoresist can be exposed through the lower, thin, gate conductor and shadowed by the thick gate conductor in their self-aligned processes which expose the photoresist by directing the exposing radiation through the substrate as a means of establishing the channel region gap between the source and drain electrodes in a self-aligned manner. Transmission of the exposing (UV) radiation through the first, thin gate conductor layer may be provided by use of a conductor layer which is transparent to that light frequency or alternatively, by use of gate metallization material which is opaque to that light frequency, but whose thickness is kept below about 100 Å whereby a substantial portion of the actinic radiation incident thereon passes therethrough.

In this alternative process, the gate metallization pattern is fabricated in the same manner as described above and the device fabrication carried out in the manner described above through the deposition of the layer of intrinsic amorphous silicon. Next, a layer of dielectric material is deposited on that amorphous silicon layer. Then a positive photoresist layer is disposed on that layer of dielectric material, exposed to actinic radiation through the substrate and the underlying layers of the device being fabricated and developed. This leaves a plug of photoresist in alignment with the thick, upper conductor of the gate metallization. This plug is then used as a mask for the removal of the dielectric layer where it is not protected by the photoresist. This leaves a plug of the dielectric material disposed on the intrinsic amorphous silicon in alignment with the thick, upper gate conductor material. Since this plug is set back from the edge of the gate electrode (the outer edge of the lower thin gate conductor) and will eventually space the source and drain electrodes apart, the overlap between the source and drain electrodes and the gate is substantially greater than it is in those basic processes for the same photoresist exposure and development conditions. Consequently, there will in general be no need to overexpose or overdevelop the photoresist in order to increase that overlap between the gate electrode and the source and drain electrodes.

Next, a layer of n^+ doped amorphous silicon is deposited over the dielectric plug and the exposed portions of the intrinsic amorphous silicon. The source/drain metallization is then deposited, a planarization layer such as photoresist is formed over the upper surface of the structure and that upper surface of the structure is uniformly etched in a non-selective manner until the source/drain metallization is exposed over the dielectric plug because of its greater height there. This exposed portion of the source/drain metallization may then be selectively etched to expose the n^+ doped amorphous silicon which is disposed on the dielectric plug. The now exposed portion of the n^+ amorphous silicon is then removed to expose the top of the dielectric plug to isolate the source and drain electrodes from each other in this region. The source/drain metallization layer is then further patterned to remove at least those portions which connect the source and drain electrodes to each other outside this portion of the structure. Alternatively, that patterning of the source/drain metallization may be done before deposition of the planarization layer. Any other steps necessary to the fabrication of the device are then carried out.

There are a number of other variations possible. The silicon could be left unpatterned. This results in intrinsic amorphous silicon and n^+ amorphous silicon being left under the source/drain metallization in all places. For applications such as imagers this is acceptable. Just the intrinsic amorphous silicon could be patterned before the n^+ amorphous silicon deposition and then the source/drain metallization deposited. This would result in n^+ under the source/drain metallization in all places. This could be acceptable even for displays where the contact to the transparent electrode would then be metal/ n^+ /transparent electrode.

While the invention has been described in detail herein in accord with certain preferred embodiments thereof, many modifications and changes therein may be effected by those skilled in the art. Accordingly, it is intended by the appended claims to cover all such modifications and changes as fall within the true spirit and scope of the invention.

What is claimed is:

1. A method of fabricating a thin film transistor comprising the steps of:
 - depositing a first gate conductor layer on a major surface of a substrate;
 - depositing a second gate conductor layer over said first gate conductor layer, said second gate conductor layer being susceptible to etching under conditions under which said first gate conductor layer is substantially immune to etching;
 - providing a photoresist layer over said second gate conductor layer;
 - exposing and developing said photoresist in a pattern in accordance with a desired configuration of said first gate conductor layer;
 - etching said second gate conductor layer and said first gate conductor layer where they are not protected by the retained portion of said photoresist layer; then
 - etching back, with an etchant to which said first gate conductor layer is substantially immune, said second gate conductor layer to expose peripheral portions of said first gate conductor layer in a self aligned manner so as to form a patterned gate electrode having a gate conductor topology wherein said second gate conductor layer has sloped side-

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walls set back a selected overlap distance from sidewalls of said first gate conductor layer, said selected overlap distance corresponding to the exposed peripheral portions of said first gate conductor layer;

removing any remaining photoresist;

depositing over said substrate and said first and second gate conductor layers a substantially conformal gate dielectric layer, depositing over said gate dielectric layer a substantially conformal semiconductor material layer, and depositing over said semiconductor material layer a substantially conformal source/drain metallization layer such that said gate conductor topography is propagated upward through each of said layers;

applying a planarization layer over said source/drain metallization layer;

planarizing said planarization layer to expose at least a portion of said source/drain metallization layer disposed over and corresponding to an uppermost portion of said patterned gate conductor topography; and

etching said source/drain metallization layer to form self-aligned source and drain electrodes disposed over said first gate conductor layer at least by said selected overlap distance.

2. The method recited in claim 1 wherein said first gate conductor layer is substantially transparent to at least one frequency in the infrared-to-ultraviolet portion of the electromagnetic spectrum.

3. The method recited in claim 1 wherein: said semiconductor material is silicon.

4. The method recited in claim 1 wherein:

said semiconductor material is amorphous silicon.

5. A method of fabricating a thin film transistor comprising the steps of:

depositing a first gate conductor layer on a major surface of a substrate;

depositing a second gate conductor layer over said first gate conductor layer, said second conductor being susceptible to etching under conditions under which said first gate conductor layer is substantially immune to etching;

providing a photoresist layer over said second gate conductor layer;

exposing and developing said photoresist in a pattern in accordance with a desired configuration of said first gate conductor layer;

etching said second gate conductor layer and said first gate conductor layer where they are not protected by the retained portion of said photoresist layer; then

etching back, with an etchant to which said first gate conductor layer is substantially immune, said second gate conductor layer to expose peripheral portions of said first gate conductor layer in a self-aligned manner so as to form a patterned gate electrode having a gate conductor topology wherein said second gate conductor layer has sloped sidewalls set back a selected overlap distance from sidewalls of said first gate conductor layer, said selected overlap distance corresponding to the exposed peripheral portions of said first gate conductor layer;

depositing a substantially conformal dielectric layer over said patterned gate conductor and exposed portions of said substrate upper surface;

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depositing a substantially conformal layer of semiconductor material over said dielectric layer;

depositing a layer of source/drain metallization over said semiconductor material layer;

forming a planarization layer of a planarization material over the source/drain metallization, said planarization layer having a substantially planar exposed surface;

uniformly removing said planarization material until said source/drain metallization is exposed in alignment with raised portions of said second gate conductor layer; and

selectively removing the exposed source/drain metallization to expose the underlying semiconductor material layer such that the remaining source/drain metallization is disposed over said patterned gate conductor by at least said selected overlap distance.

6. The method recited in claim 5 wherein:

the step of depositing the layer of semiconductor material comprises:

first depositing a layer of substantially undoped semiconductor material; and

second depositing a layer of doped semiconductor material; and

said method further comprises, after the step of selectively removing the source/drain metallization, the step of:

removing the doped semiconductor material portion of said semiconductor material layer.

7. The method recited in claim 6 wherein:

said semiconductor material is silicon.

8. The method recited in claim 7 wherein:

said semiconductor material is amorphous silicon.

9. The method recited in claim 5 wherein:

said semiconductor material is silicon.

10. The method recited in claim 9 wherein:

said semiconductor material is amorphous silicon.

11. The method recited in claim 5 further comprising the step of:

providing a back channel passivation layer over the structure.

12. The method recited in claim 5 wherein said first gate conductor layer is substantially transparent to at least one frequency in the infrared-to-ultraviolet portion of the electromagnetic spectrum.

13. A method of fabricating a thin film transistor comprising the steps of:

depositing a first gate conductor layer on a major surface of a substrate, said first gate layer being transmissive of at least one frequency of radiation capable of exposing photoresist;

depositing a second gate conductor layer over said first gate conductor layer, said second conductor layer being opaque to said at least one frequency of radiation and being susceptible to etching under conditions under which said first gate conductor layer is substantially immune to etching;

providing a photoresist layer over said second gate conductor layer;

exposing and developing said photoresist in a pattern in accordance with a desired configuration of said first gate conductor layer;

etching said second gate conductor layer and said first gate conductor layer where they are not protected by the retained portion of said photoresist layer; then

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etching back, with an etchant to which said first gate conductor layer is substantially immune, said second gate conductor layer to expose peripheral portions of said first gate conductor layer in a self-aligned manner so as to form a patterned gate electrode having a gate conductor topology wherein said second gate conductor layer has sloped sidewalls set back a selected overlap distance from sidewalls of said first gate conductor layer, said selected overlap distance corresponding to the exposed peripheral portions of said first gate conductor layer;

depositing a first substantially conformal dielectric layer over said patterned gate conductor and exposed portions of said substrate upper surface;

depositing a substantially conformal layer of semiconductor material on said dielectric layer;

depositing a second layer of photoresist on the second dielectric layer;

exposing a back-side substrate surface, opposite to said major substrate surface, to UV light for a selected duration, to cause exposure of at least a portion of the second photoresist layer outside of a shadow of the opaque portion of said gate electrode;

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removing at least the exposed second photoresist portion by selective development, to form a mask for etching the second dielectric layer;

etching said second dielectric layer to remove the portions not protected by the retained portion of said second photoresist;

depositing a layer of doped semiconductor material on the exposed semiconductor portion and over the remaining portion of the second dielectric layer;

depositing a layer of source/drain metallization over said doped semiconductor material layer;

forming a planarization layer of a planarization material over the source/drain metallization, said planarization layer having a substantially planar exposed surface;

uniformly removing said planarization material until said source/drain metallization is exposed in alignment with raised portions of said patterned gate conductor; and

selectively etching the exposed portion of the source/drain metallization and a portion of the doped semiconductor layer, to expose at least a top surface of the remaining portion of said second dielectric layer, and to form self-registered source and drain electrodes each of which overlaps the gate electrode at least by said selected overlap distance.

* * * * *

EXHIBIT I-4



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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------------|------------------|
| 10/184,118 | 06/28/2002 | Moo Yeol Park | 8733.631.00 | 9942 |
| 30827 | 7590 | 06/19/2006 | | |
| MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006 | | | EXAMINER PAIK, STEVE S | |
| | | | ART UNIT 2876 | PAPER NUMBER |

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | | | |
|------------------------------|------------------------|----------------|---------------------|--|--|
| Office Action Summary | Application No. | | Applicant(s) | | |
| | 10/184,118 | | PARK ET AL. | | |
| | Examiner | | Art Unit | | |
| | | Steven S. Paik | 2876 | | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 31 March 2006.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1,2,4-10,13-17 and 19-22 is/are rejected.

7) ☒ Claim(s) 3,11,12,18,23 and 24 is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 24 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some * c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

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| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____. |
|--|--|

Application/Control Number: 10/184,118

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 31, 2006 has been entered.

Response to Amendment

2. Receipt is acknowledged of the Amendment filed March 31, 2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 13, 14, 16, 17 and 19-22 are rejected under 35 U.S.C. 103(a) as being obvious over Egami et al. (US 6,304,311) in view of Jeong (US 6,573,968).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of

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07-176-TJW**

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invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Re claims 1, 2 and 21, Egami discloses a method of manufacturing a liquid crystal display (LCD) device comprising the steps of preparing a lower substrate (3) and an upper substrate (6), applying a liquid crystal on one of the lower and upper substrates (col. 2, ll. 17-33), attaching the lower and upper substrates, and curing at least the main sealant (col. 4, ll. 7-37) Ultraviolet rays (8) are irradiated for curing the sealants.

Egami fails to explicitly disclosing the step of forming auxiliary sealants formed in a dummy region and connects to the main sealant or extends outside from the main sealant.

Jeong discloses a seal pattern that includes a plurality of main seal lines (210), a first auxiliary seal lines (220) including a plurality of first openings, a second auxiliary seal line (230), and a plurality of third auxiliary seal lines (240). As figure 8 discloses there is connection between auxiliary seal lines (240a, 240b). The third auxiliary seal lines pass only gas such as air and the main seal lines are protected from being damaged from a cleaning detergent or an etchant during a cleaning and etching process.

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Thus, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to further incorporate the step of forming a plurality of auxiliary seals (210-240) formed in a dummy region (outside the main seal 210) and connecting to the main sealant (through an opening 212), as taught by Jeong to the method of manufacturing a liquid crystal display device of Egami due to the fact that main seals can be protected from a cleaning detergent or an etchant during a cleaning and etching process.

Re claim 13, Egami in view of Jeong disclose the method as recited in rejected claim 2 stated above, wherein the UV light (8) is irradiated at a tilt angle (see Fig. 1E of Egami) with respect to the attached substrates (3 and 6).

Re claim 14, Egami in view of Jeong disclose the method as recited in rejected claim 1 stated above, further comprising forming column spacers (14) on the upper substrates (col. 1, ll. 14-20).

Re claims 16 and 17, Egami in view of Jeong disclose the method as recited in rejected claim 1 stated above, further comprising cutting the attached substrates (col. 1, ll. 63+).

Re claims 19 and 20, Egami in view of Jeong disclose the method as recited in rejected claim 1 stated above, wherein the applying the liquid crystal includes dropping the liquid crystal onto the one of the upper and lower substrates. The liquid crystal is poured into respective panels (Fig. 4A-4D).

Re claim 22, Egami in view of Jeong disclose the method as recited in rejected claim 21 stated above, wherein the UV light (8) is irradiated at a tilt angle (see Fig. 1E) with respect to the attached substrates (3 and 6).

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07-176-TJW

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4. Claims 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egami (US 6,304,311) as modified by Jeong (US 6,573,968) as applied to claim 2 above, and further in view of Yamanaka (US 6,146,927).

The teachings of Egami in view of Jeong have been discussed above. Egami in view of Jeong disclose a method of manufacturing a liquid crystal display (LCD) device comprising the steps of preparing at least two substrates, providing a plurality of sealants, and bonding said substrates together.

However, neither Egami nor Jeong specifically disclose the specific characteristics about the sealants.

Yamanaka discloses an LCD comprises a liquid crystal driving device 11 and the color filter substrate CF which are combined through a sealer 13 (epoxy or acrylic ultraviolet irradiation/heat curing adhesive) therebetween, and a liquid crystal C sealed between an oriented film 12 provided on the side of the liquid crystal driving device 11 and an oriented film 12' provided on the side of the color filter substrate CF (col. 24, ll. 5-25). As appreciated by an artisan in the art, the sealer may be an epoxy or acrylic group depends on how the sealants are cured. One may use both an epoxy and acrylic group in accordance with a particular substrate of the LCD device.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have selected either an epoxy or acrylic group sealant or both an epoxy and acrylic group sealant based on the substrates of LCD to be bonded and a method of curing the sealants. Such selection would simplify the process of curing the sealants and improve the adhesiveness of the substrates having a particular property.

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5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Egami (US 6,304,311) as modified by Jeong (US 6,573,968) as applied to claim 2 above, and further in view of Wakita et al. (USPN 5,307,190).

The teachings of Egami in view of Jeong have been discussed above. Egami in view of Jeong disclose a method of manufacturing a liquid crystal display (LCD) device comprising the steps of preparing at least two substrates, providing a plurality of sealants, and bonding said substrates together.

Both of the aforementioned references fail to teach the main and auxiliary sealants are formed on upper substrates and the liquid crystal is applied to the lower substrate.

Wakita discloses a method of manufacturing liquid crystal display (LCD) comprises the steps of loading a first substrate having liquid crystal arranged thereon (col. 4, line 54) and a second substrate having sealant coated thereon (ultraviolet-curable sealant on a peripheral portion of at least one of substrates) into a bonding chamber (vacuum chamber) and bonding the first and second substrates by varying an applied pressure (pressing the substrates in a vacuum chamber; col. 7, ll. 14-41).

In view of Wakita reference, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to further incorporate the separate application process of the sealants on one substrate and the liquid crystal on the other substrate in addition to the method of fabricating an LCD of Egami modified by Jeong due to the fact that the separate application, which can be performed at the same time, would increase the speed of manufacturing process.

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Allowable Subject Matter

6. Claims 3, 11, 12, 18, 23, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: none of the cited prior arts of the record discloses, a method of manufacturing an LCD, comprising, among other steps, contiguous main and auxiliary sealant and providing a mask over a region where the main sealant is not formed before irradiating UV light such that the auxiliary sealant is not exposed to the UV light and cutting the attached substrates.

Additional Remarks

8. Upon reviewing the applicant's Request for Continued Examination and further search of prior art, it is concluded that previously allowed claims 1-20 and 23 are not allowable. The examiner regrets any delay caused by this Office Action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven S. Paik whose telephone number is 571-272-2404. The examiner can normally be reached on Monday - Friday 5:30a-2:00p (Maxi-Flex*).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 571-272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.


LPL 003338
07-176-TJW

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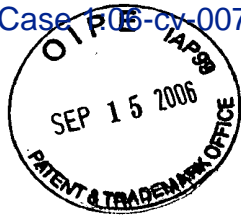
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Steven S. Paik
Primary Examiner
Art Unit 2876

ssp

LPL 003339
07-176-TJW

EXHIBIT I-5



Docket No. 8733.631.00-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Moo Yeol PARK et al.

Confirmation No.: 9942

Application No.: 10/184,118

Art Unit: 2876

Filed: June 28, 2002

Examiner: Steve S. Paik

For: LIQUID CRYSTAL DISPLAY DEVICE AND
METHOD OF MANUFACTURING THE
SAME

Customer No.: 30827

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated June 19, 2006, please amend the patent application identified above as follows:

INTRODUCTORY COMMENTS

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 5 of this paper.

DC:50424843.1

**LPL 003380
07-176-TJW**

Application No.: 10/184,118

Docket No.: 8733.631.00-US

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of manufacturing a liquid crystal display (LCD) device comprising:
 - preparing a lower substrate and an upper substrate;
 - forming an auxiliary sealant and subsequently forming a main sealant on one of the lower and upper substrates, wherein the auxiliary sealant is formed in a dummy region and connects to the main sealant, and wherein the auxiliary sealant and the main sealant are contiguous;
 - applying a liquid crystal on one of the lower and upper substrates;
 - attaching the lower and upper substrates; and
 - curing at least the main sealant.
2. (Original) The method of claim 1, wherein the main sealant and the auxiliary sealant are at least partially curable by irradiating UV light and curing the main sealant includes irradiating UV light.
3. (Cancelled)
4. (Original) The method of claim 2, wherein the sealant is formed using oligomers each having both ends coupled to an acrylic group.
5. (Original) The method of claim 2, wherein the sealant is formed using monomers each having both ends coupled to an acrylic group.
6. (Original) The method of claim 2, wherein the sealant is formed using oligomers each having one end coupled to an acrylic group and the other end coupled to an epoxy group.
7. (Original) The method of claim 2, wherein the sealant is formed using monomers each having one end coupled to an acrylic group and the other end coupled to an epoxy group.

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8. (Original) The method of claim 2, further comprising heating the sealant after irradiating the UV light.

9. (Original) The method of claim 6, further comprising heating the sealant after irradiating the UV light.

10. (Original) The method of claim 7, further comprising heating the sealant after irradiating the UV light.

11. (Original) The method of claim 2, wherein a region where the sealant is not formed is covered with a mask during the irradiating with UV light.

12. (Original) The method of claim 2, wherein a region where the main UV sealant is not formed is covered with a mask during the irradiating with UV light.

13. (Original) The method of claim 2, wherein the UV light is irradiated at a tilt angle with respect to the attached substrates.

14. (Original) The method of claim 1, further comprising forming column spacers on the upper substrate.

15. (Original) The method of claim 1, wherein the main and auxiliary sealants are formed on the upper substrate and the liquid crystal is applied to the lower substrate.

16. (Original) The method of claim 1, further comprising cutting the attached substrates.

17. (Original) The method of claim 16, wherein the attached substrates are cut across a portion of the auxiliary sealant.

Application No.: 10/184,118

Docket No.: 8733.631.00-US

18. (Original) The method of claim 2, further comprising:
providing a mask over a region where the main sealant is not formed before irradiating UV light such that the auxiliary sealant is not exposed to the UV light; and
cutting the attached substrates.
19. (Original) The method of claim 1, wherein the applying the liquid crystal includes dropping the liquid crystal onto the one of the upper and lower substrates.
20. (Original) The method of claim 19, wherein the liquid crystal is applied in a predetermined pattern onto the one of the upper and lower substrates.
21. (Currently Amended) A method of manufacturing a liquid crystal display (LCD) device comprising:
preparing a lower substrate and an upper substrate;
forming an auxiliary UV sealant and a main UV sealant on one of the lower and upper substrates, wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant, wherein the auxiliary UV sealant contacts the main UV sealant;
applying a liquid crystal on one of the lower and upper substrates;
attaching the lower and upper substrates; and
irradiating UV light on the attached substrates.
22. (Original) The method of claim 21, wherein the UV light is irradiated at a tilt angle with respect to the attached substrates.
23. (Previously Presented) The method of claim 1, wherein the auxiliary sealant contacts the main sealant.
24. (Cancelled)

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Docket No.: 8733.631.00-US

REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Office Action dated June 19, 2006 has been received and its contents carefully reviewed. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 3, 11, 12, 18, 23 and 24.

By this Amendment, claims 1 and 21 are amended and claims 3 and 24 are cancelled without prejudice or disclaimer. Accordingly, claims 1, 2 and 4-23 are currently pending in the present application.

In the Office Action, the Examiner rejected claims 1, 2, 13, 14, 16, 17 and 19-22 under 35 U.S.C. § 103(a) as being unpatentable over Egami et al. (U.S. Patent No. 6,304,311) in view of Jeong (U.S. Patent No. 6,573,968); rejected claims 4-10 under 35 U.S.C. § 103(a) as being unpatentable over Egami et al. and Jeong in view of Yamanaka (U.S. Patent No. 6,146,927); and rejected claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Egami et al. and Jeong in view of Wakita et al. (U.S. Patent No. 5,307,190).

Although Applicants respectfully traverse the aforementioned rejections, for the sole purpose of expediting the prosecution of the present application, claims 1 and 21 are amended. In particular, claim 1 as amended includes the allowed subject matter of claim 3 and claim 21 as amended includes the allowed subject matter of claim 24. Claims 2, 4-20 and 23 depend from claim 1 and claim 22 depend from claim 21. Accordingly, Applicants respectfully submit that all pending claims, claims 1, 2 and 4-23, are in condition for immediate allowance.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the

Application No.: 10/184,118

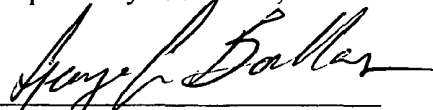
Docket No.: 8733.631.00-US

filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: September 15, 2006

By



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Washington, DC 20006
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EXHIBIT S-2

Digital
Multimedia
Standards
Series

DIGITAL VIDEO: AN INTRODUCTION TO MPEG-2



Barry G. Haskell,
Atul Puri, and
Arun N. Netravali

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where `horizontal_size` is the width of the image in terms of pels and the `vertical_size` is the height of the image in lines. As an example consider a 4:3 IAR display, and suppose the image width is 720 pels and the image height is 486 lines. Then PAR can be calculated as follows.

$$\text{PAR} = 4/3 \times 486/720 = 0.9$$

In the second case, PAR is calculated as follows:

$$\text{PAR} = \text{IAR} \times \frac{\text{display_vertical_size}}{\text{display_horizontal_size}}$$

This second case is signalled via `sequence_display_extension()` which carries information regarding `display_horizontal_size` and `display_vertical_size` which determine the size of the display rectangle. When this display rectangle is smaller than the image size it implies that only a portion of image is to be displayed, and conversely when the display rectangle is larger than the image size it implies that the image is displayed only on a portion of the display screen.

It is worth noting that computer displays use square pels ($\text{PAR} = 1.0$) and if material intended for TV is shown on a computer display, correction of the pel aspect ratio is necessary; otherwise, circles on a TV screen appear as ellipses on a computer display.

5.1.5 Gamma

Many TV cameras and all CRT-based displays have a nonlinear relationship between signal voltage and light intensity. The light intensity input to the camera or output by the display is proportional

to the voltage raised to the power gamma and is given by the following generalized relationship:

$$B = cv^\gamma + b$$

where B is the light intensity, v is voltage, c is a gain factor, b is either cutoff (camera) or black level (cathode ray tube, CRT) light intensity, and γ typically takes values in the range of 1 to 2.5, although for some picture displays it can be as high as 3.0.

Typically, camera picture tubes or CCD sensors have a gamma of about 1 except for a vidicon type picture tube, which has a gamma of 1.7. The CRT displays use kinescopes, which typically have a gamma of 2.2 to 2.5.

To avoid gamma correction circuitry inside millions of TV receivers, gamma correction is done prior to transmission. For example, assuming the gamma of the camera to be 1 and that of the display to be 2.2, then the camera voltage is raised to a power of $1/2.2 = 0.45$. *(Isn't gamma mean the inverse?)*

The result of gamma correction is that a gamma-corrected voltage is generated by the camera that can be transmitted and applied directly to the CRT. As a side benefit, the gamma-corrected voltage is also less susceptible to transmission noise.

In normal TV transmission, the signal from the camera is gamma corrected, modulated, and transmitted to the receiver as a radiofrequency (RF) signal, which is received by the receiver's antenna and demodulated and applied to the display. The main components of such a TV transmission system are shown in Fig. 5.4.

In our discussion thus far, we have considered only monochrome TV and have deferred a discussion about color TV so that we could introduce

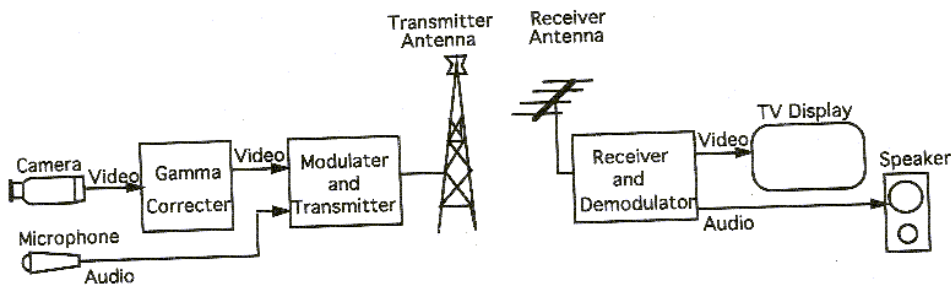


Fig. 5.4 Monochrome television analog transmission system

some aspects of human vision and how they are exploited in the design of a color TV system.

5.2 THE HUMAN VISUAL SYSTEM AND COLOR TV

With the background on video imaging developed thus far, we are now well prepared to delve into the intricacies of the human visual system, the perception of color, the representation of color, and further to specific color TV systems.

5.2.1 The Human Visual System

The human eye is a remarkably intricate system; its anatomy is shown in Fig. 5.5.

Incoming light bouncing off different objects is refracted by the cornea toward the pupil. The pupil is the opening of the iris through which all light enters the eye. The light again is refracted by the lens onto the back of the eyeball, forming an image on the retina. The retina consists of receptors sensitive to light called photoreceptors connected by nerve cells. To reach these photoreceptors, light must first pass through nerve cells. The photoreceptors contain chemical pigments that can absorb light and initiate a neural response. There are two types of photoreceptors, rods and cones. Rods are responsible for low light vision, while cones are responsible for details and color under normal light conditions, as in daylight. Both rods and cones enable vision when the amount of light is between the two extremes. Light absorbed by photoreceptors initiates a chemical reaction that bleaches the pigment, which reduces the sensitivity to light in proportion to amount of pigment bleached. In general, the amount of bleached pigment rises or falls depending on the amount of light. The visual information from the retina is passed via optic nerves to the brain. Beyond the retina, processing of visual information takes place en route to the brain in areas called the lateral geniculate and the visual cortex. Normal human vision is binocular, composed of a left-eye and a right-eye images. The left-eye image is processed by the right half of the brain, and the right-eye image by the left half of brain. We further discuss

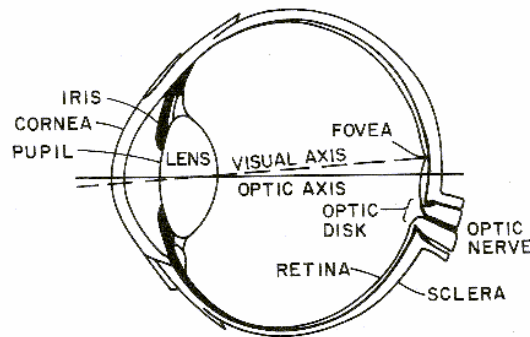


Fig. 5.5 Anatomy of the human eye

the intricacies of the human visual system, and in particular as it refers to binocular vision, in Chapter 15.

Light of various wavelengths produces a sensation called *color*. Different distributions generally result in the perception of different colors. A color is thus visible energy of a given intensity and of a given composition of wavelengths. The normal human visual system can identify differences in sensation caused by different colors and thus colors can be classified. In our earlier discussion of the human visual system we mentioned that the retina of the human eye contains photoreceptors called cones that are responsible for color vision. The human retina contains a color-sensitive area that consists of three sets of cones that are individually sensitive to red, green, and blue light. Thus the sensation of color experienced directly depends on the relative amounts of red, green, and blue light; for instance, if only blue and red cones are excited, the sensation is magenta. When different combinations of red, blue, and green cones are excited, different colors are sensed; a combination of approximately 30% red, 60% green, and 10% blue results in white light.

5.2.2 Hue and Saturation

The sensation known as color produced by visible light is also called *hue*. Visible light is electromagnetic radiation with a spectrum of wavelengths; a hue is determined by its dominant wavelength. Besides hue, *saturation* is another property of interest and represents the degree of

purity of a color or having a sing 100%, while the is zero. The th *brightness, hue, a* defined by its amplitude versus er discussion ab by the response cones in the reti that the perceiv ors is exactly th response from th na. The trich implies that hue or can be dupli tion of the thre

5.2.3 Co

One of the many colors is t sen such as to : and saturation three primaries color primaries maries and the maries. Subtra photography, a maries are usec

Although a additive mixtu observers matc in the amount the color arise dard observer averaging the (ber of observ chromaticity d region in whic or and is ide Three such pc triangle form gamut of colo play using the has defined th color primari three such po

EXHIBIT S-3

PRENTICE

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INTERNATIONAL

EDITIONS

DIGITAL LOGIC CIRCUIT ANALYSIS AND DESIGN

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BILL D. CARROLL

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TABLE 5.4 BINARY-TO-GRAY CODE TRUTH TABLE

| Decimal Number | Binary $B_3B_2B_1B_0$ | Gray Code $G_3G_2G_1G_0$ |
|----------------|--------------------------|-----------------------------|
| 0 | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0011 |
| 3 | 0011 | 0010 |
| 4 | 0100 | 0110 |
| 5 | 0101 | 0111 |
| 6 | 0110 | 0101 |
| 7 | 0111 | 0100 |
| 8 | 1000 | 1100 |
| 9 | 1001 | 1101 |
| 10 | 1010 | 1111 |
| 11 | 1011 | 1110 |
| 12 | 1100 | 1010 |
| 13 | 1101 | 1011 |
| 14 | 1110 | 1001 |
| 15 | 1111 | 1000 |

5.4.3 Lookup Tables

A common application of PROMs is the *lookup table*, in which a function is stored in tabular form with its arguments used as an index into the table to retrieve the value of the function for those arguments. Since truth tables can be readily realized by PROMs, lookup tables are implemented by writing them in truth table format and then realizing the truth table with a PROM. Tables of trigonometric functions, logarithms, exponentials, and other functions can thus be easily implemented. In addition, numerical calculations that can be tabularized, such as addition, subtraction, and multiplication, can also be readily implemented with PROMs, as illustrated in the following example.

EXAMPLE 5.9

Implement an 8-bit by 8-bit high-speed binary multiplier to compute

$$P_{15-0} = A_{7-0} \times B_{7-0}$$

using PROMs as lookup tables to perform all arithmetic operations.

Rather than using a single large PROM with 16 inputs and 16 outputs to implement a multiplication table with 2^{16} rows, let us partition the two operands

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into 4-bit quantities as follows.

$$\begin{aligned}
 P_{15-0} &= A_{7-0} \times B_{7-0} \\
 &= ((A_{7-4} \times 2^4) + A_{3-0}) \times ((B_{7-4} \times 2^4) + B_{3-0}) \\
 &= (A_{7-4} \times B_{7-4}) \times 2^8 + ((A_{7-4} \times B_{3-0}) + (A_{3-0} \times B_{7-4})) \times 2^4 \\
 &\quad + A_{3-0} \times B_{3-0}
 \end{aligned}$$

This operation can be done with four 4-bit by 4-bit multipliers to compute partial products and three binary adders to add the partial products. The multiplications by 2^4 and 2^8 can be done by simply shifting the corresponding terms 4 and 8 bits, respectively, to the left. Note that the multiplication table for a 4-bit by 4-bit multiplication has only 16 rows.

The block diagram of Fig. 5.26 is a system of PROMs used to implement the multiplier. PROMs 1 to 4 are programmed as multiplication lookup tables

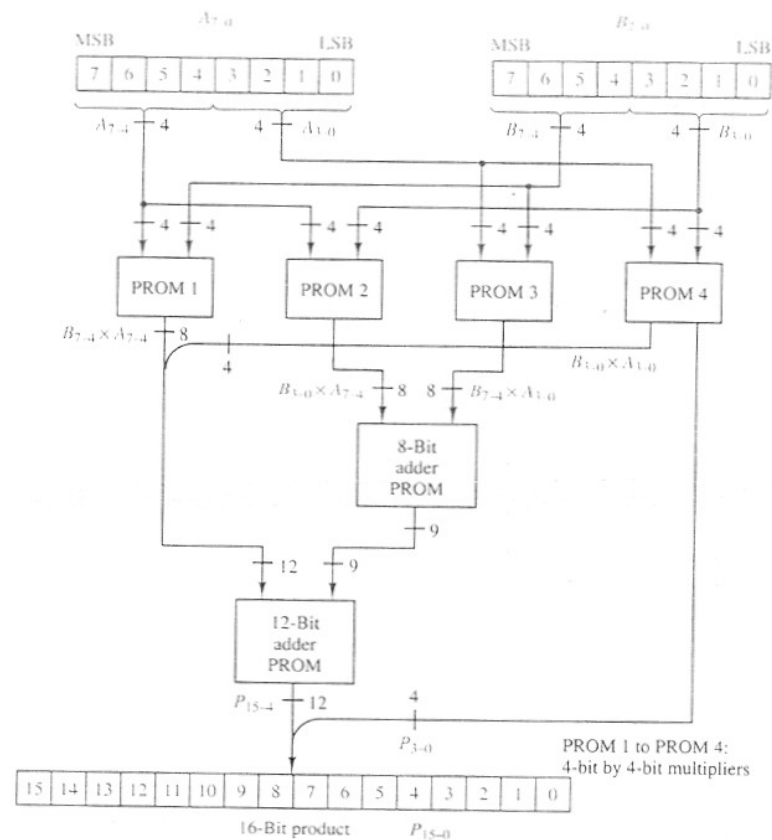


Figure 5.26 Implementation of a high-speed binary multiplier with PROMs. (PROMs 1 to 4 are 4×4 multipliers).



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EXHIBIT U-2



US006043591A

United States Patent [19]

Gleckman

[11] Patent Number: 6,043,591

[45] Date of Patent: *Mar. 28, 2000

[54] LIGHT SOURCE UTILIZING DIFFUSIVE REFLECTIVE CAVITY

[75] Inventor: Philip L. Gleckman, Irvine, Calif.

[73] Assignee: Teledyne Lighting and Display Products, Inc., Hawthorne, Calif.

[*] Notice: This patent is subject to a terminal disclaimer.

[21] Appl. No.: 08/923,207

[22] Filed: Sep. 4, 1997

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/131,659, Oct. 5, 1993, Pat. No. 5,440,197.

[51] Int. Cl.⁷ G02F 1/133

[52] U.S. Cl. 313/110; 359/619

[58] Field of Search 313/110; 362/19, 362/26, 257; 359/619, 622, 625-626

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Primary Examiner—Thomas D. Lee

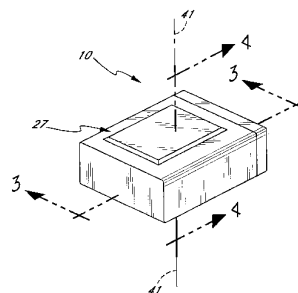
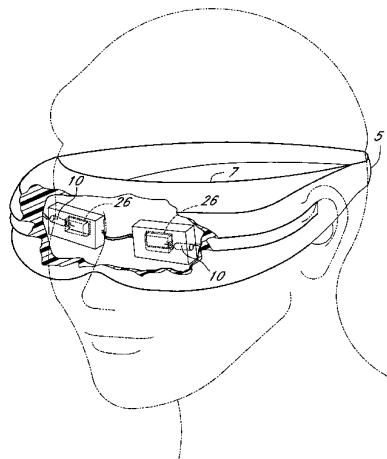
Assistant Examiner—Stephen Brinich

Attorney, Agent, or Firm—Knobbe, Martens, Olson & Bear, LLP

[57] ABSTRACT

A light source for backlighting a display comprises a light-emitting device such as an incandescent bulb or LED array disposed within a cavity having diffusely reflecting walls and an aperture. A diffuser and brightness enhancing film are situated at the opening of the aperture between the aperture and the display to be backlit. A color filter may also be employed to whiten the light emerging from the light source.

18 Claims, 6 Drawing Sheets



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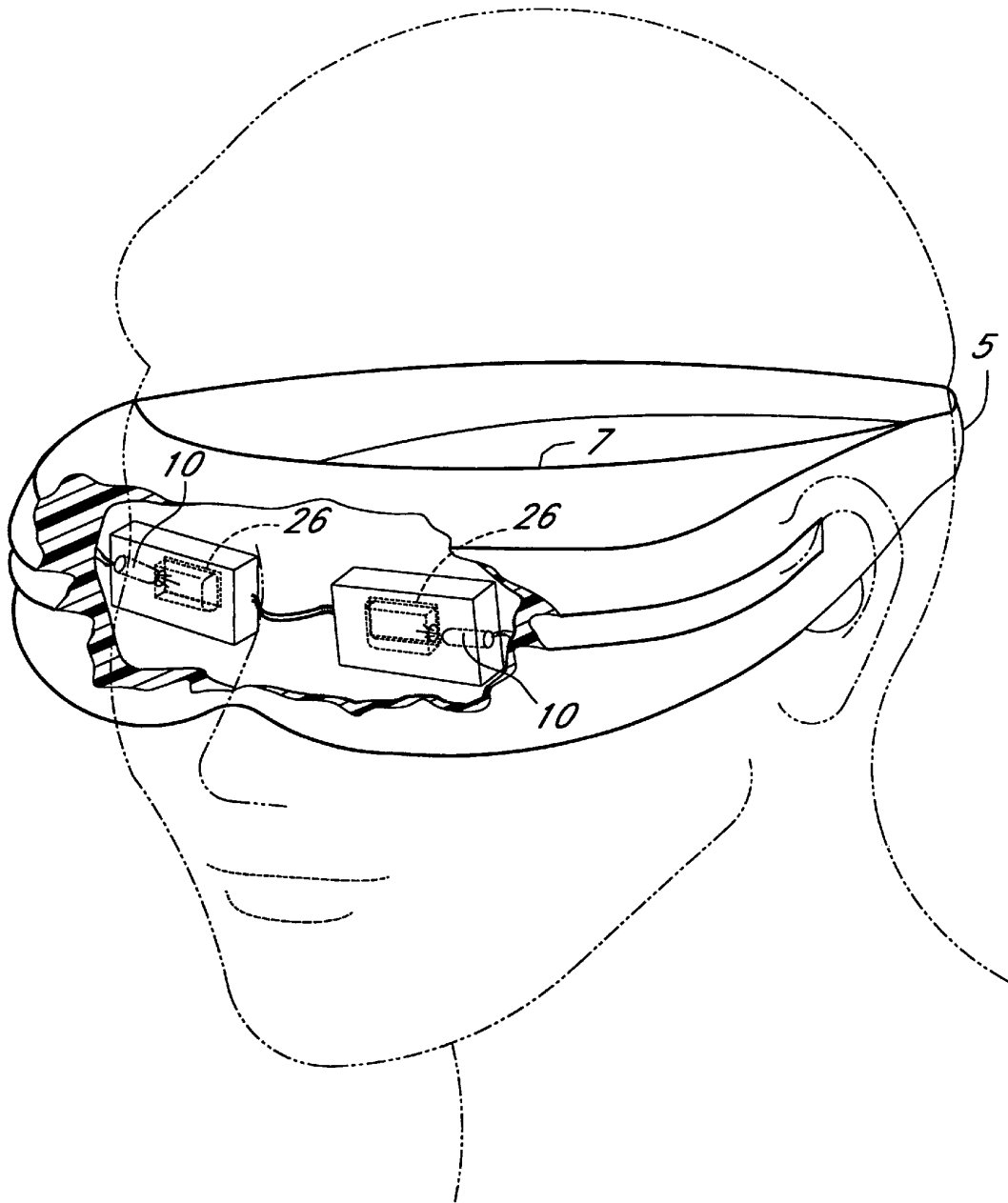
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FIG. 1

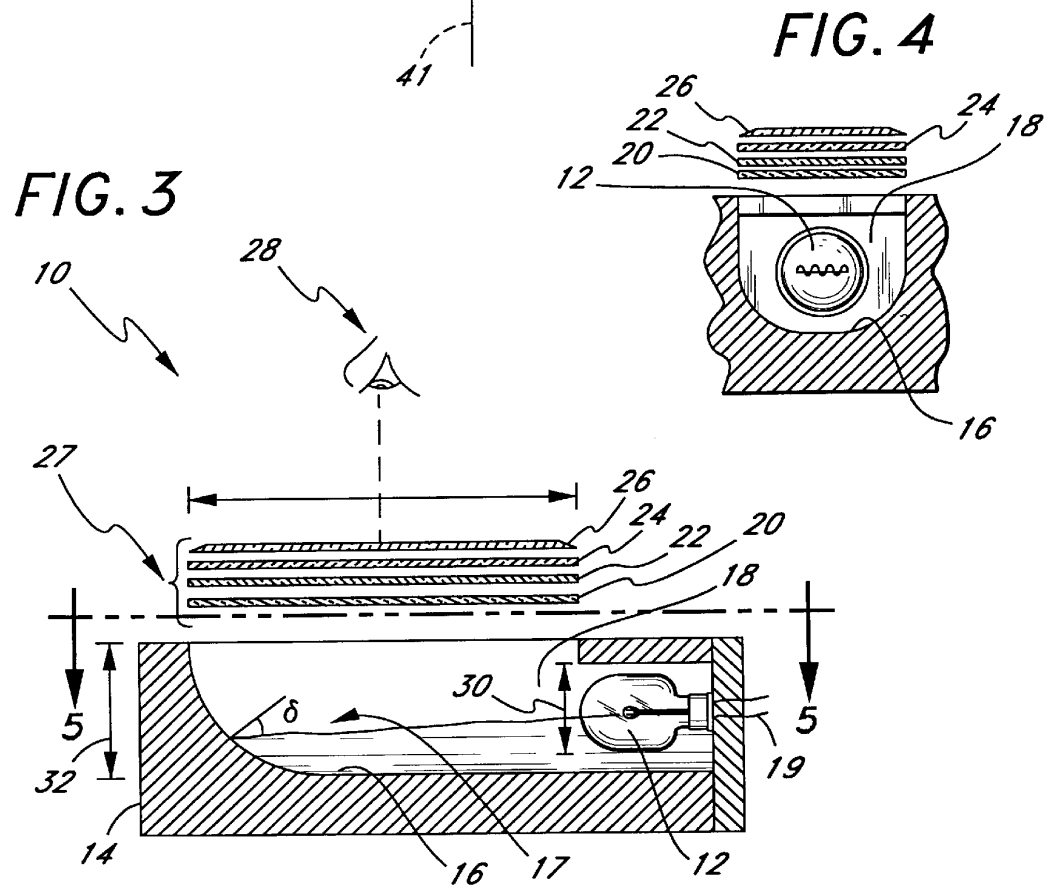
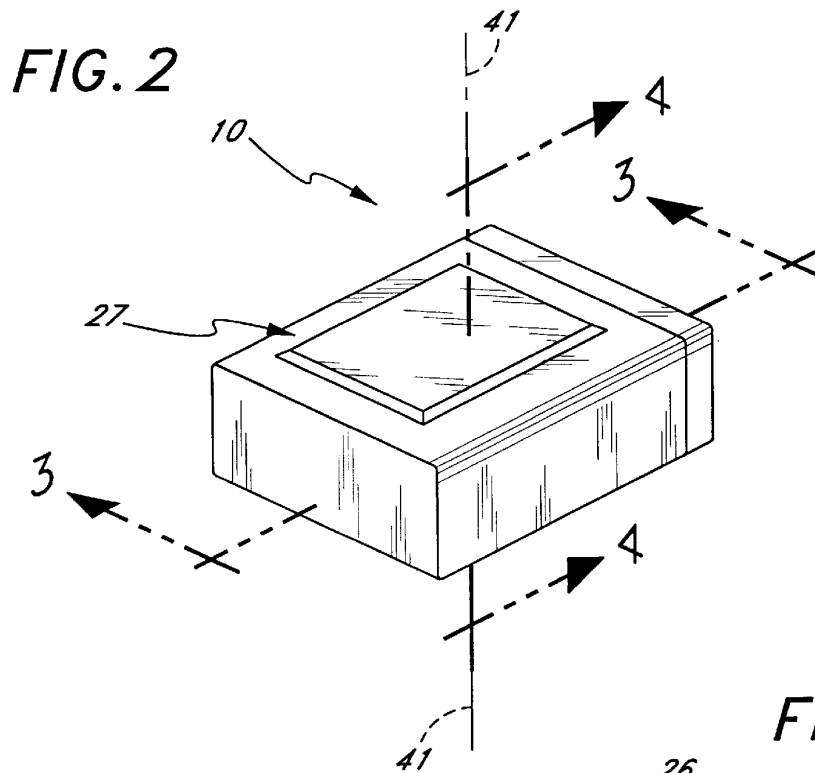


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FIG. 5

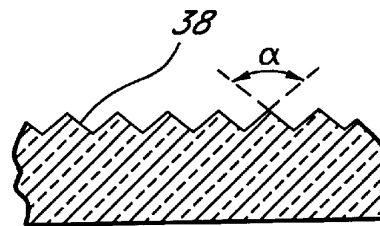
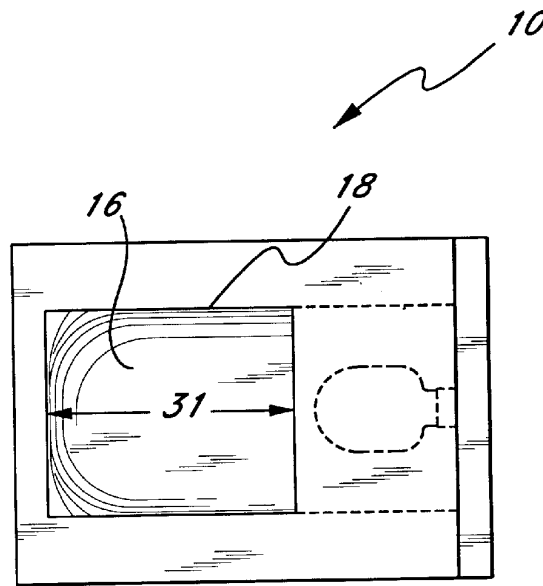
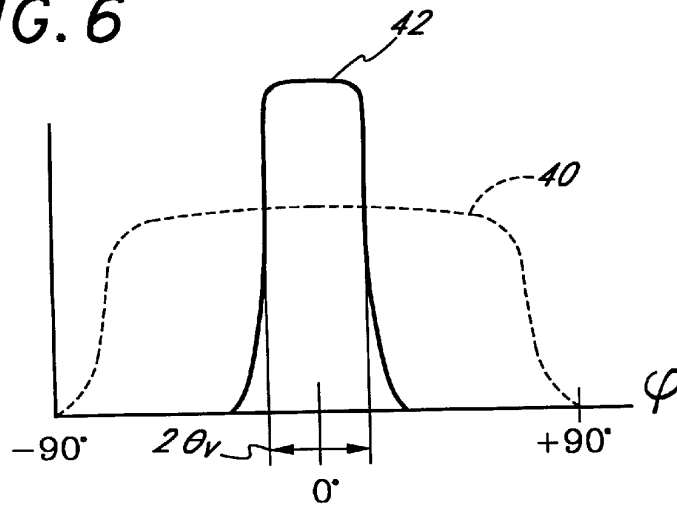


FIG. 7

FIG. 6

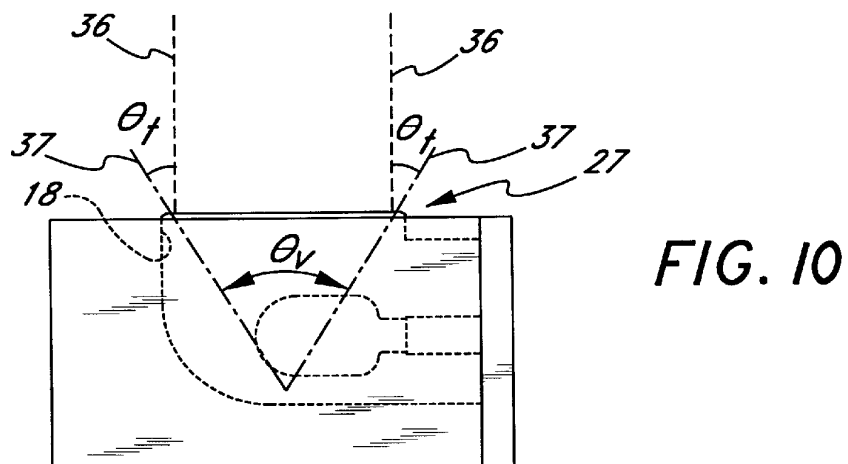
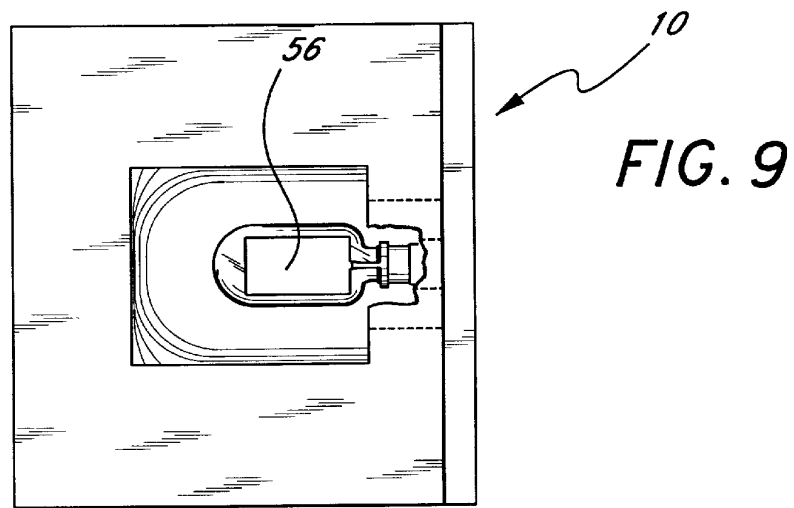
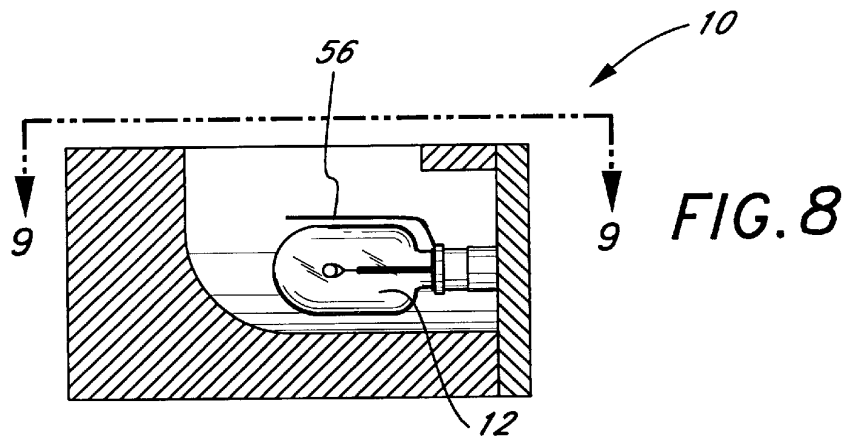


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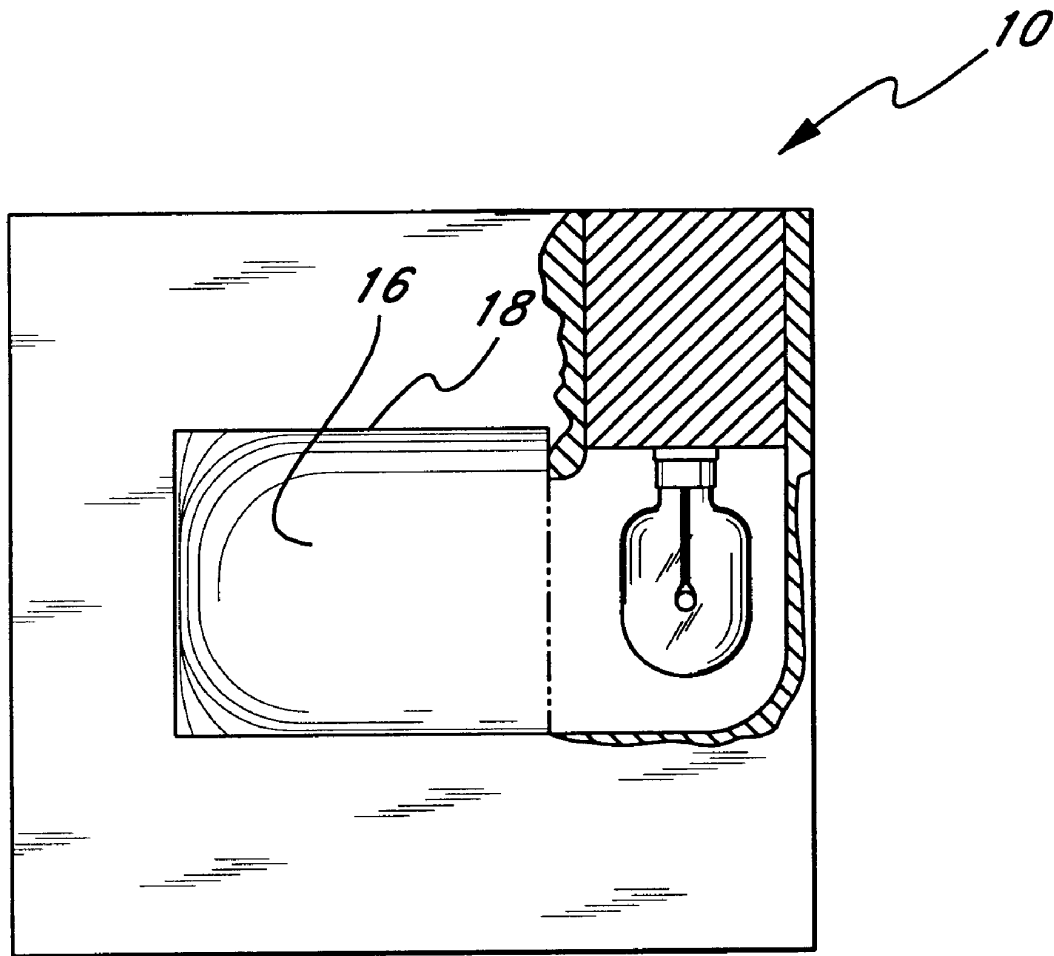


FIG. II

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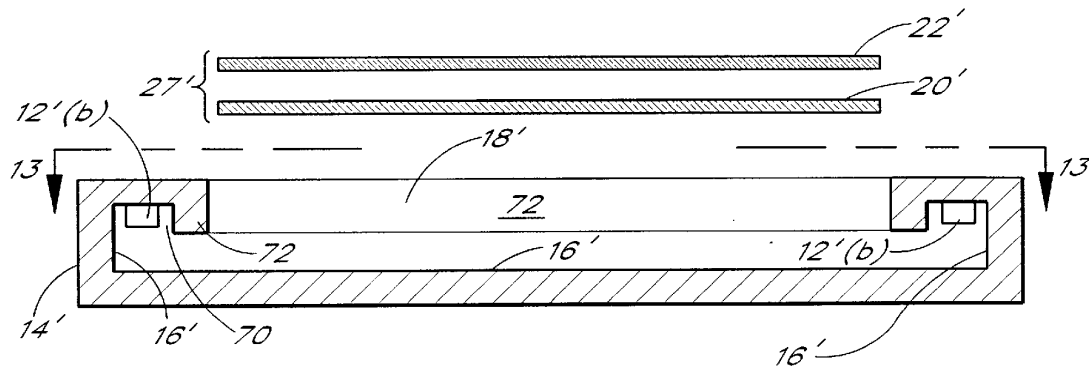


FIG. 12

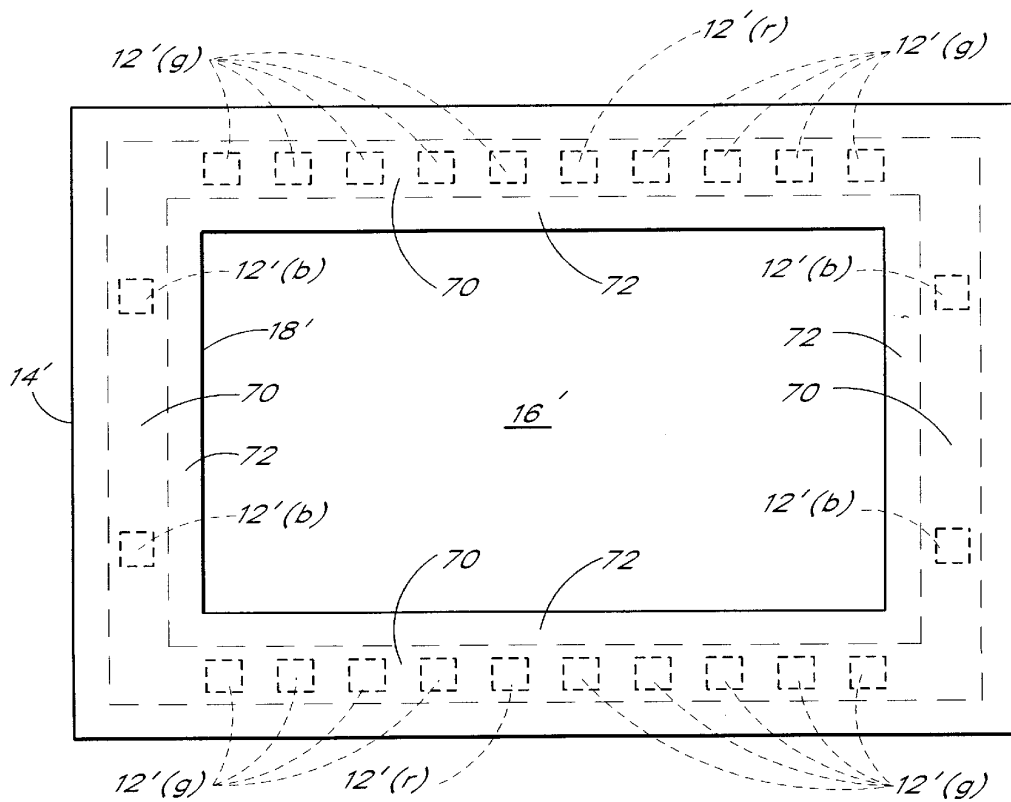


FIG. 13

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LIGHT SOURCE UTILIZING DIFFUSIVE REFLECTIVE CAVITY

This application is a continuation in part of application Ser. No. 08/131,659, filed Oct. 5, 1993 now U.S. Pat. No. 5,440,197.

BACKGROUND OF THE INVENTION

The present invention relates to a backlighting apparatus for displays, particularly for small-area liquid-crystal displays (LCDs), such as utilized in virtual reality headsets. LCDs, which allow the display of alphanumeric, graphic or other information, may comprise a medium whose transmittance changes in response to the application of an electrical potential across the medium. The LCDs may be viewed even in an otherwise dark environment by applying illumination uniformly to their rear face. An exemplary backlighting apparatus for an LCD is disclosed in U.S. Pat. No. 4,043,636.

It is desirable for a backlight for small-area LCDs, such as those found in helmets of virtual reality systems, to have certain attributes. Firstly, it must have an acceptable level of brightness. Secondly, it is preferable to have a spectral distribution that is as white as possible, particularly if the LCDs display color images. The light source must be compact, and preferably require little maintenance. Lastly and most importantly, the lighting system must provide uniform illumination across the entire area of the display. This latter need translates into a requirement that the light emerging from the light source be featureless and free of distortions such as holes or rings. In practice, the requirement of uniform illumination is difficult to achieve, and prior art devices frequently fail to provide a sufficiently uniform source of illumination for LCD displays. Additionally, prior art devices frequently relied on light guides to direct light to reflective surfaces, necessitating complicated geometries and added weight and expense.

An object of the present invention is therefore to provide a simple, compact, lightweight means for backlighting a display, typically a small-area LCD display, which provides highly uniform, high-intensity illumination of the entire display panel.

SUMMARY OF THE INVENTION

The light source of the present invention backlights a rear surface of a display panel, and includes a housing having diffusely reflective interior surfaces which form a cavity. A device that emits light, for example, an incandescent light bulb or LED array, is mounted in the cavity with the interior surfaces of the cavity spaced therefrom. The housing has an aperture juxtaposed with the rear surface of the display panel which opens into the cavity. The ratio of the area of the aperture to the sum of (i) the area of said aperture and (ii) the diffusely reflective surface area of the cavity is at least 0.05 in a preferred embodiment of the present invention. The ratio of the depth of the cavity to an edge to edge dimension of the aperture is at least 0.1. The aperture of the embodiment disclosed also has a bisector dimension, defined as the edge-to-edge length of the aperture along a line formed by the intersection of the plane of the aperture and a plane normal to the plane of the aperture extending through the bulb and bisecting the aperture. The ratio of the depth of the cavity to its bisector dimension is at least 0.1 in a preferred embodiment of the present invention. In one embodiment of the present invention, the depth of the cavity is not substantially greater than the diameter of the envelope of the light bulb.

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The light source also comprises a diffuser placed across the aperture and positioned to diffuse illumination which passes through the aperture from the cavity toward the display panel. A brightness enhancing material for passing illumination within a viewing range is disposed between the diffuser and the display panel. In a preferred embodiment having orthogonally oriented brightness enhancing films, the viewing range is 50 degrees. This range is the sum of a pair of angles of 25 degrees measured relative to lines normal to the plane of the aperture.

If desired, a color filter may be included between the cavity and the LCD. In the preferred embodiment, the filter is placed between the brightness enhancing film (BEF) and the rear surface of the display to increase the color temperature of the light incident on the display.

In one embodiment of the present invention, the light bulb is positioned in a portion of the cavity that is outside of a viewing aperture portion, so that the filament is not visible through the aperture within the viewing angle. In another embodiment of the present invention, the light bulb is located within the viewing aperture portion of the cavity beneath the aperture. A baffle in front of the lamp reflects light towards the bottom of the cavity, and prevents the bulb from directly emitting illumination through the aperture thereby preserving the uniformity of the light emerging from the aperture. In yet another embodiment, the light is produced by an LED array. The LEDs have colors (e.g. red, blue, and green) and intensities which produce, in combination, light that is white in color.

In all embodiments, the emitted light is diffusely reflected within the interior surfaces of the cavity, such that the cavity effectively functions as a lambertian light source. The diffuser gives the transmitted light a more uniform intensity distribution. The brightness enhancing film (BEF) concentrates the light emerging from the diffuser by projecting it into a smaller angular viewing range, and thereby enhances the intensity within the viewing angle. Finally, a color filter, which is typically blue for incandescent light, may be used to change the color temperature of the incandescent light from 2800K–3300K to around 4500K–5500K, thereby providing a whiter color.

The invention also encompasses a method of backlighting a display panel comprising the step of producing illumination from a substantially lambertian light source having a cavity with internal walls and an aperture. The producing step comprises the step of directing light rays from the perimeter of the aperture into the cavity such that the light exiting the aperture is substantially uniform in intensity and color. The method also includes the steps of using a diffuser to diffuse light from the substantially lambertian light source using a brightness-enhancing film to concentrate the diffused light into a predetermined angular range without significantly reducing the uniformity of the diffused light, and directing the concentrated diffused light onto the display panel.

The backlighting apparatus of the present invention produces illumination of a very uniform character, with relatively high intensity and whiteness, in a device that is both simple and compact.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a virtual reality headset incorporating an LCD backlit by the light source of the present invention.

FIG. 2 is a perspective view of an embodiment of the light source of the present invention.

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FIG. 3 is a cross-sectional view of the light source of FIG. 2 taken along the lines 3—3 of FIG. 2.

FIG. 4 is an end-on cross-sectional view of the light source of FIG. 2 taken along the lines 4—4 of FIG. 2.

FIG. 5 is a plan view of the light source of FIG. 2 taken along the lines 5—5 of FIG. 3.

FIG. 6 is a graph showing the intensity of light emitted from the light source shown in FIGS. 2 as a function of viewing angle.

FIG. 7 is a fragmentary view in cross section, of a brightness enhancing film as shown in FIG. 3.

FIG. 8 is a cross sectional view of a second embodiment of the present invention.

FIG. 9 is a plan view of the embodiment of FIG. 8.

FIG. 10 is a schematic view of the light source showing the viewing angle.

FIG. 11 is a plan view of an alternate embodiment of the light source which is identical in all respects to the embodiment of FIG. 2 except that the light source is mounted transversely to the configuration depicted in FIG. 2.

FIG. 12 is a cross-sectional view of an embodiment utilizing an arrangement of red, blue, and green LEDs which in combination produce white light.

FIG. 13 is a plan view of the light source of FIG. 12 taken along the lines 13—13 of FIG. 12.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

As shown in FIG. 1, one preferred embodiment of the present invention comprises a virtual reality headset 5 configured to be worn on the head of a user. The headset 5 has a pair of small-area color display panels 26 disposed within an interior cavity 7 of the headset. Each of the panels 26 comprises an LCD with a front face and a rear face of identical size. Each of the front faces of the panels 26 is positioned behind an eyepiece (not shown) that is directly in front of a respective eye of the user so that each eye views the front face of a single one of the panels. By way of example, each of the faces of the display panels 26 is rectangular, having a length of $\frac{1}{2}$ " and a width of $\frac{1}{2}$ ". The headset is configured to fit against the face of the user sufficiently tightly so that light from ambient sources cannot enter the cavity 7. When properly mounted on the user's head, the headset will always be in substantially the same position relative to the user's face, and the display panels 26 will thus also always be in substantially the same position with respect to the user's eyes. Accordingly, each time the headset is worn, the eye of the viewer will have the same viewing position with respect to the display screens 26.

Each of the panels 26 includes a backlighting apparatus 10, as shown in FIGS. 2 and 3. The backlight 10 is comprised of a bulb 12, located within a housing 14 having an aperture 18, covered by a diffuser 20, a brightness enhancing film (BEF) 22, and a color filter 24. The diffuser 20, BEF 22, and color filter 24 are placed in physical contact with each other, forming a planar structure hereinafter referred to as a light quality enhancing (LQE) apparatus 27. The LCD display 26, which is backlit by light emerging through the aperture 18 from cavity surfaces 16, is juxtaposed with the LQE apparatus 27, so that the display 26 may be viewed from a position 28. Although the headset 5 has not been shown in FIG. 2 for clarity of illustration, it will be understood that the position 28 would be within the interior cavity 7 of the headset 5.

In one embodiment of the present invention, the housing 14 has lateral internal dimensions of 13 mm×33 mm, and the

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thickness or depth of the housing is 10 mm, slightly larger than the diameter of a standard flashlight bulb. The aperture 18 is 13 mm square in this embodiment. The aperture 18 is preferably smaller than 2 inches square to ensure uniform illumination of the cavity walls 16 opposite the aperture 18 by the incandescent bulb 12.

The lamp 12 is preferably an incandescent light bulb such as a common flashlight lamp powered by a power source (not shown) connected to wires 19. The lamp 12 is preferably entirely enclosed in the housing 14 so that only the wires 19 emerge from the housing 14. The wires 19 pass through a small passageway in a wall of the housing 14. The passageway is just large enough to accommodate the wires 19 and is substantially smaller than the diameter of the bulb, thereby minimizing light leakage emanating from the annular space, if present, between the wires and the housing 14.

Light radiating from the lamp 12 propagates within the housing 14, which forms a cavity comprising diffusely reflecting interior surfaces 16 preferably having a reflectivity of at least 88%. The surfaces 16 may be coated with white paint or more exotic materials such as the Labsphere Corporation's Spectrafect paint. Spectrafect paint's reflectivity is considerably higher than house paint, roughly 98%, while the reflectivity of house paint is approximately 92%. Additionally, the housing 14 may be entirely constructed from a diffusely reflecting material, such as TiO_2 pigmented Lexan™ polycarbonate or Spectralon™ plastic, thereby avoiding the need to apply a separate coating to the interior surfaces 16 of the housing 14. The reflectivity of Spectralon™ plastic is about 99%.

Light emerging from the lamp 12 typically undergoes several reflections within the cavity formed by the housing 14 before eventually emerging from the aperture 18. Because the interior surfaces 16 of the housing 14 are diffusely reflecting, the multitude of diffuse reflections cause the interior surface of the housing 14 opposite the aperture 18 to be uniformly lit and act as a substantially lambertian source, i.e., a light source having the property that the radiance or brightness of the interior cavity surfaces is constant as a function of viewing angle.

In constructing the light source 10 of the present invention, there are a number of factors to consider. One of these is the area of the aperture 18. Another is the combined cavity area, that is the sum of (i) the surface area of the cavity interior 16 and (ii) the area of the aperture 18. For maximally efficient use of the energy emitted from the bulb 12 and uniformity of the emitted light from the aperture 18, it is important that the ratio of the area of aperture 18 to the combined cavity area be relatively high to ensure minimal energy loss within the light source. Preferably, this ratio is at least 0.05, and in the preferred embodiment the ratio is close to 0.20. Referring to FIG. 4, the side cavity walls 16 are curved; such an arrangement decreases the combined cavity area, and thus increases the aforementioned ratio of the area of the aperture to the combined cavity area. The bottom cavity wall may also be curved as well to decrease the angle δ (shown in FIG. 3) as a function of increasing distance from the bulb. The angle δ is the angle formed between a line drawn from the filament of the bulb 12 and the outward-pointing normal to a plane tangent to the cavity surface at each point.

Another parameter of importance shown in FIG. 5, is the edge-to-edge dimension 31 of the aperture 18, referred to herein as the bisector dimension. This bisector dimension extends along a line formed by the juncture of the plane of the aperture and a plane normal to the plane 41 of the

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aperture 18 extending through the bulb 12 and bisecting the aperture. The ratio of the depth of the housing 14 to this bisector dimension affects both the intensity and uniformity of the light visible through the opening of the aperture 18. If this ratio is too large, the aforementioned ratio of the area of the aperture to the combined cavity area becomes too small. With a small ratio, light from bulb 12 will also undergo fewer reflections from the cavity walls 16 and undergo $1/r^2$ fall off, resulting in a less-uniform intensity distribution. In the preferred embodiments of the present invention, the ratio is more than approximately 0.10.

Still another parameter of the present invention is the ratio of the diameter 30 of the envelope of the lamp 12 (typically the width of the bulb) to the depth 32 of the cavity formed by the housing 14. In the preferred embodiment of the present invention, this ratio is sufficiently high to achieve compactness. The housing 14 is preferably constructed so that the depth 32 is not substantially greater than the diameter 30 of the bulb. By way of example, the ratio may be 0.60.

While the housing 14 and the aperture 18 basically function as a source of uniform light intensity even in the absence of the diffuser 20, in the preferred embodiment of present invention the diffuser 20 is advantageously placed in the opening of the aperture 18 to remove residual nonuniformities such as cosmetic imperfections in the interior surfaces 16 of the cavity. The diffuser is comprised of translucent material, typically a readily available thin plastic surface or volume diffuser. Both of these materials are preferred because they are characterized by very low absorption, thus minimizing energy losses.

To avoid wasting optical energy, it is preferable to match the numerical aperture of the backlight with the numerical aperture of the optics (e.g., the eyepiece of the headset 5) that receives the light from the backlight. Because the cavity acts as a substantially lambertian source, it is necessary to decrease the numerical aperture of the backlight, and thereby concentrate the light emanating from the aperture. In particular, the backlight 10 employs the BEF 22 placed between the diffuser 20 and the display 26 to concentrate the illumination, and thereby increases the brightness.

It is helpful for present purposes to define an angle which characterizes the performance of BEF 22. This angle, θ_c (shown at 39 in FIG. 10), is the semi-angle from a normal 36 to the plane of the aperture 18. More specifically, the BEF 22 transmits light rays within θ_c . Except for weak side lobes, no light will be transmitted by the BEF beyond the angle θ_c .

A second angle, the viewing angle θ_v , shown at 41, subtends twice the angle θ_c of the BEF 22. Consequently, $\theta_v = 2\theta_c$.

It will be understood that concentration of the illumination by the BEF 22 (within the angle θ_c), shown in FIG. 10, is symmetrical only in the sense that concentration occurs within a plane coincident with the plane of the paper in FIG. 10. The BEF 22 does not provide concentration within the orthogonal plane. In some applications of the invention, it is preferable to concentrate the illumination in both of the orthogonal planes. This may be accomplished by including a second BEF oriented orthogonally to the BEF shown in FIG. 10. Such an arrangement would provide a boundary line 37 at each of the four edges of the aperture 18 and thereby concentrate the illumination so that substantially no radiation beyond the angle θ_c is transmitted from the aperture 18.

Referring to FIG. 7, the BEF of the preferred embodiment is a commercially available thin film having linear pyrami-

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dal structures 38. In principle, the structures 38 transmit only those rays from the cavity that satisfy the incidence angle criteria for transmission into the transmission region bounded by the boundary lines 37. All other rays will be reflected back into the cavity, where they are diffusely reflected again by the cavity walls. In effect, the reflected rays are "recycled" until they are incident on the BEF at an angle which permits them to pass through the BEF into the transmission region.

The fraction f of light retroreflected by the pyramidal structures 38 of the BEF 22 satisfies the relationship $1-f=\sin \theta_c$. The brightness-enhancing effect results from the fact that many of the retroreflected rays are themselves diffusely reflected and eventually are transmitted by the BEF 22. Because the BEF 22 is designed so that $\theta_c < 90$ degrees, it concentrates light within the display range, thereby increasing the intensity of light seen within this range. Using pyramidal structures, a 40% gain over an unenhanced lambertian source has been observed. If a film having orthogonally oriented rows is used, a gain of as much as 80% may be possible. The use of orthogonally oriented films produces the enhancing effect in two orthogonal planes rather than only along the axis perpendicular to the pyramidal structures, as is the case when only one set of pyramidal structures 38 is used. In the preferred embodiment, the structure of the film is sufficiently fine that it is imperceptible to the viewer of the display 26 and the light intensity resulting therefrom is as uniform as possible. Referring to FIG. 7, the BEF 22 may be a film having an apex angle α (typically about 100°). Such film is available from 3M. As an alternative to two orthogonally oriented lenticular films of the type shown in FIG. 7, an array of two-dimensional micro lenses may be utilized.

The concentrating effect of the BEF 22 is depicted in FIG. 6, which is a graph of the brightness of light observed as a function of viewing angle ϕ (here, viewing angle ϕ is defined as the angle the eye of the observer makes with the plane of the aperture 18). Graph 40 illustrates the intensity as a function of viewing angle without the BEF 22, while graph 42 shows a distribution achieved with the BEF 22. It can be seen that the intensity achieved within the window $\theta_v = 2\theta_c$, degree wide is greater than that achieved by use of the diffuser alone. It is also important to note that the BEF is placed between the diffuser and the display, since the latter has a spreading effect on the angular distribution of light, while the former concentrates it.

FIG. 6 also illustrates an advantageous feature of the present invention, namely the uniformity of the distribution of illumination throughout the viewing range 60. It can be seen that the graph 42 of the light intensity emerging from the BEF 22 as a function of viewing angle ϕ is highly uniform throughout the entire viewing angle θ .

Light emerging from the BEF 22 passes through the color filter 24 in a preferred embodiment of the present invention. The color temperature of the flashlight bulb that comprises the lamp 12 is only about 2800K. However, color LCD displays require a higher color temperature to achieve ideal color purity. Consequently, when an incandescent source is employed as the lamp 12, a filter may be used to shift the color distribution as desired. The filter 24 of the preferred embodiment is a blue absorbing filter that shifts the color temperature to between about 4500K and 5500K. Light passing through the filter 24 continues through the LCD 26 to the eye of the viewer located at the position 28. The gaps between elements 20, 22, and 24 in FIG. 1 are depicted only for clarity; the thicknesses of and separation between each of the various elements are minimized for the sake of compactness.

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In the embodiment of the backlight illustrated in FIGS. 2–3, the lamp 12 is situated in the housing 14 so that it is outside of a viewing aperture portion 17. As used herein, the term “viewing aperture portion” refers to the portion of the cavity that lies directly beneath the aperture 18. Placement of the lamp 12 outside the viewing aperture portion 17 prevents most of the light rays emanating from the lamp 12 from reaching the aperture 18 without first being reflected off a surface of the cavity. Since only glancing rays from the bulb 12 directly impinge on the LQE 27 and the diffuser 20 scatters these rays, this arrangement allows the intensity distribution of light emerging from the aperture 18 to be relatively uniform. An alternate embodiment of the backlighting system allowing even more compact construction is illustrated in FIGS. 8–9, in which corresponding numbers denote like parts. The lamp 12 is placed in a different portion of the housing 14. In this embodiment, the lamp 12 is placed directly within the viewing aperture portion 17. The lamp 12 is shielded from the aperture 18 by an opaque baffle 56. The baffle 56 has two diffusely reflecting outer surfaces which are coated with one of the diffusely reflecting materials described above. The diffusely reflecting surfaces of the baffle 56 prevent the lamp 12 from directly illuminating the aperture 18, while reflecting light incident thereon, such as any rays reflected back toward the aperture from the diffuser and the BEF, thus preserving the uniformity of the light distribution. Since the lamp 12 is directly beneath the aperture, as opposed to being set back in the housing 14 outside viewing aperture 17, the housing 14 can be more laterally compact than that of the embodiment of FIG. 2. Additionally, the embodiment of FIG. 8 allows a higher ratio of the aperture surface area to the combined cavity area, thus allowing even greater efficiency in the use of energy emanating from the bulb 12. Aside from this placement of the lamp, all details of this embodiment, such as the coating of the interior surfaces of the housing 14 and the placement of the diffuser, BEF and filter, are identical to those of FIG. 2.

A further embodiment, illustrated in FIG. 11, is identical to the embodiment shown in FIGS. 1–5, except for the orientation of the bulb 12. Accordingly, like numbers designate like parts. In the embodiment of FIG. 11, the bulb is oriented so that a line extending along its longitudinal axis is parallel to, but spaced from, the aperture (as opposed to the embodiment shown in FIG. 5, where a line extending along the longitudinal axis of the bulb passes beneath the aperture). Thus, the bulb in FIG. 11 is rotated 90° relative to the bulb in FIG. 5.

Yet another embodiment of a lambertian light source is shown in FIGS. 12 and 13. In this embodiment, red, blue, and green light from light emitting diodes (LED) is mixed together in a manner well known in the art to produce white light. For clarity of illustration, parts corresponding to like parts of prior embodiments will be designated using like numbers that are primed. As illustrated, a housing 14' comprises a diffusively reflecting cavity having interior cavity walls 16' and an aperture 18' which opens into the cavity. The dimensions of the aperture 18' are 16.1 mm by 14.1 mm for the particular arrangement shown, which uses 2 red LEDs 12'(r), 4 blue LEDs 12'(b), and 18 green LEDs 12'(g). As shown in FIG. 13, the LEDs are mounted around the periphery of the aperture 18' within a channel 70 that extends around the entire perimeter of the aperture 18'. The channel 70 is formed by a small baffle 72 that extends from the edge of the aperture 18 a short distance into the cavity and along the entire perimeter of the aperture 18'. Preferably, the distance by which the baffle 72 extends into the cavity is no greater than is necessary to prevent the LEDs from being

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viewed through the aperture 18'. In any event, the baffle 72 is spaced from the cavity walls 16 by a sufficient distance to permit light from the LED's to diffusively reflect into the portion of the cavity beneath the aperture 18'. In preferred embodiments, the depth of the cavity is 5–10 mm. As is typical of light-emitting diodes, the LEDs 12' comprise tiny cubes of solid-state material that emit light. In the embodiment shown, the solid-state material is not encased in a housing, and no directional reflectors are used such that the emission is allowed to propagate multidirectionally from plural faces of the solid-state cubes. Such multifaceted emission enhances the uniformity of the intensity of light exiting the aperture 18'.

The LEDs 12' are positioned so that for each color (red, blue, green) the output from the aperture 18' is substantially uniform with respect to intensity. In the preferred embodiment, the LEDs 12' are positioned symmetrically, with an equal number of diodes 12' of like color on opposite edges of the rectangular aperture 18'. Thus, as viewed from FIG. 13, the top edge of the aperture 18' has nine green diodes 12'(g) and one red diode 12'(r), while the bottom edge of the aperture also has nine green diodes 12'(g) and one red diode 12'(r). Similarly, the left edge of the aperture has two blue diodes 12'(b), while the right edge also has two blue diodes 12'(b). In addition to symmetry with respect to opposite edges of the aperture 18', the diodes preferably have substantial symmetry with respect to sides of the same edge of the aperture 18'. Thus, for example, the single red diode 12'(r) at the top edge in FIG. 13 is placed substantially in the center of that top edge with five green diodes 12'(g) on the left side and four green diodes 12'(g) on the right side. The bottom edge embodies the same symmetry except that the four green diodes are on the left side of the red diode and the five green diodes are on the right side. In regard to the left aperture edge (as seen in FIG. 13), each of the two blue diodes 12'(b) is positioned so that it is the same distance from an end of the left aperture edge as it is from the other blue diode. The blue diodes 12'(b) at the right aperture edge have this same symmetry with respect to the right aperture edge.

As mentioned above, the combination of LEDs 12' is selected to provide white light. Thus, while a diffuser 20' and BEF 22' are included, as shown in FIG. 12, no color filter is necessary because the combination of red, blue and green colors produces light of sufficient whiteness. However, in some cases it may be necessary to underdrive some of the LEDs in order to obtain the desired color balance and desired whiteness. If so, it is preferable that all LED's of the same color be underdriven by the same amount so as to preserve color uniformity at the aperture 18'. Because the illumination produced by the symmetrical arrangement of LEDs and the diffusively reflecting cavity yields a substantially uniform intensity output at the aperture 18' for each color, the light source produces a high-quality color image.

The present invention thus comprises a highly uniform, efficient, and compact light source for demanding applications such as small color LCD displays in virtual reality systems. However, it also has application in other small-area backlighting systems as well, such as in digital watches or automotive gauges. It is understood that the present disclosure of the preferred embodiment may be changed in the combination and arrangement of parts without departing from the spirit and scope of the invention hereinafter claimed.

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What is claimed is:

1. A lighting apparatus, comprising:

a device that emits light;

an optical cavity formed by diffusely reflective surfaces, said cavity having an aperture through which light from said cavity passes;

said light emitting device being mounted to supply light to said cavity while being hidden from direct view through said aperture, said cavity having a diffusely reflective surface area and said aperture having an area, the ratio of said area of said aperture to the sum of (i) said area of said aperture and (ii) said diffusely reflective surface area of said cavity being at least 0.20; and a planar optical apparatus at said aperture comprised of replicated structures configured to restrict light output from said aperture to a predetermined viewing angle.

2. The apparatus of claim 1, wherein said optical apparatus comprises a light quality enhancing (LQE) apparatus, comprising:

a diffuser at said aperture, said diffuser positioned to diffuse illumination which passes from said cavity through said aperture; and

a brightness enhancing material disposed adjacent said diffuser, said material concentrating illumination within a viewing angle so as to enhance the brightness of the display panel.

3. The apparatus of claim 1, wherein said light emitting device comprises an incandescent light bulb.

4. The apparatus of claim 1, wherein said aperture has an edge-to-edge dimension, the ratio of the depth of the cavity to said edge-to-edge dimension being at least 0.1.

5. The apparatus of claim 2, wherein said light quality apparatus additionally comprises a color filter at said aperture.

6. The apparatus of claim 3, wherein said incandescent bulb has a filament enclosed by an envelope, and wherein

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the ratio of the depth of said housing to the diameter of said envelope enclosed by said filament is less than 1.8.

7. The apparatus of claim 3, wherein said incandescent bulb has a filament enclosed by an envelope, and wherein the depth of said housing is not substantially greater than the diameter of said envelope enclosed by said filament.

8. The apparatus of claim 1, wherein the reflective surfaces of said cavity have a reflectance higher than 88 percent.

9. The apparatus of claim 1, wherein said cavity has reflective interior surfaces which comprise high-reflectance plastic.

10. The apparatus of claim 1, wherein the light emitting device comprises a fluorescent tube.

11. The apparatus of claim 2, wherein said brightness enhancing material comprises a film of linear pyramidal structures.

12. The apparatus of claim 1, wherein said viewing angle is no more than about 35 degrees.

13. The apparatus of claim 11, wherein said brightness enhancing material further comprises a second film of linear pyramidal structures disposed in a direction orthogonal to said film of linear pyramidal structures.

14. The apparatus of claim 2, wherein said diffuser is between said brightness enhancing film and said optical cavity.

15. The apparatus of claim 4, wherein said cavity is formed by interior walls of a housing.

16. The apparatus of claim 3, wherein said incandescent bulb is disposed within a viewing aperture portion of said cavity and wherein said housing further comprises a baffle positioned between the bulb and said aperture.

17. The apparatus of claim 1, wherein said aperture has straight sides, none of which exceed 2 inches in length.

18. The apparatus of claim 1, wherein the cavity is fluid filled.

* * * * *

EXHIBIT U-3



US005936353A

United States Patent [19]**Triner et al.**[11] **Patent Number:** **5,936,353**[45] **Date of Patent:** **Aug. 10, 1999**

[54] **HIGH-DENSITY SOLID-STATE LIGHTING
ARRAY FOR MACHINE VISION
APPLICATIONS**

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[75] Inventors: **James E. Triner**, Gates Mills; **Steven
D. Cech**, Aurora, both of Ohio

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[73] Assignee: **Pressco Technology Inc.**, Solon, Ohio

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[21] Appl. No.: **08/627,211**

Hewlett-Packard Co. (SnapLED), Photonics Spectra (May
1997).

[22] Filed: **Apr. 3, 1996**

[51] **Int. Cl.**⁶ **G01N 21/84; H01L 33/00**

[52] **U.S. Cl.** **315/112; 250/559.04; 257/717**

[58] **Field of Search** 315/112; 257/88,
257/99, 717; 250/559.04, 559.16, 559.17

Primary Examiner—Don Wong

Assistant Examiner—David H. Vu

Attorney, Agent, or Firm—Fay, Sharpe, Beall, Fagan,
Minnich & McKee

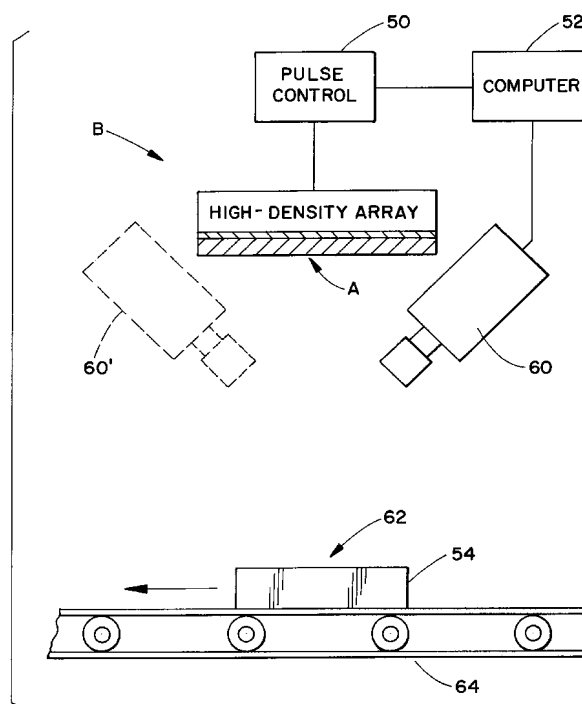
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A solid-state lighting unit for automated visual inspection includes a high-density array of light emitting diodes. The packing density of said diode array being limited only by the physical size of the light emitting diode chips and the ability to perform die and wire bond operations on the bare chips. Each diode is disposed on an electrically insulated, thermally conductive base unit. The base unit is, in turn, in a thermally conductive path with a heat dissipator. The provisions made to ensure a thermally conductive path from the individual light emitting diode chips to the heat dissipator combined with the high chip packing densities work together to create a solid-state lighting array capable of producing extremely high illumination fields when operated in either pulsed or continuous current mode.

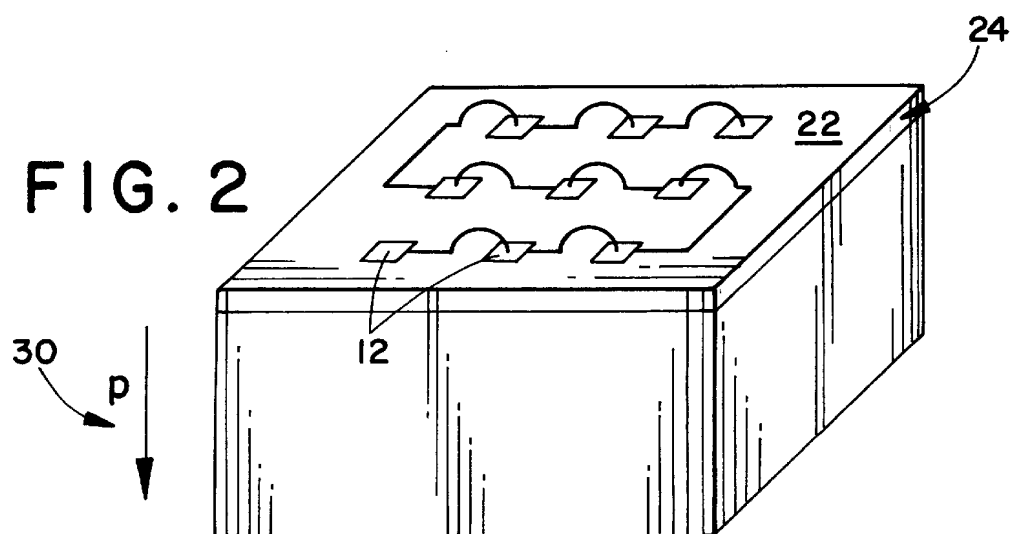
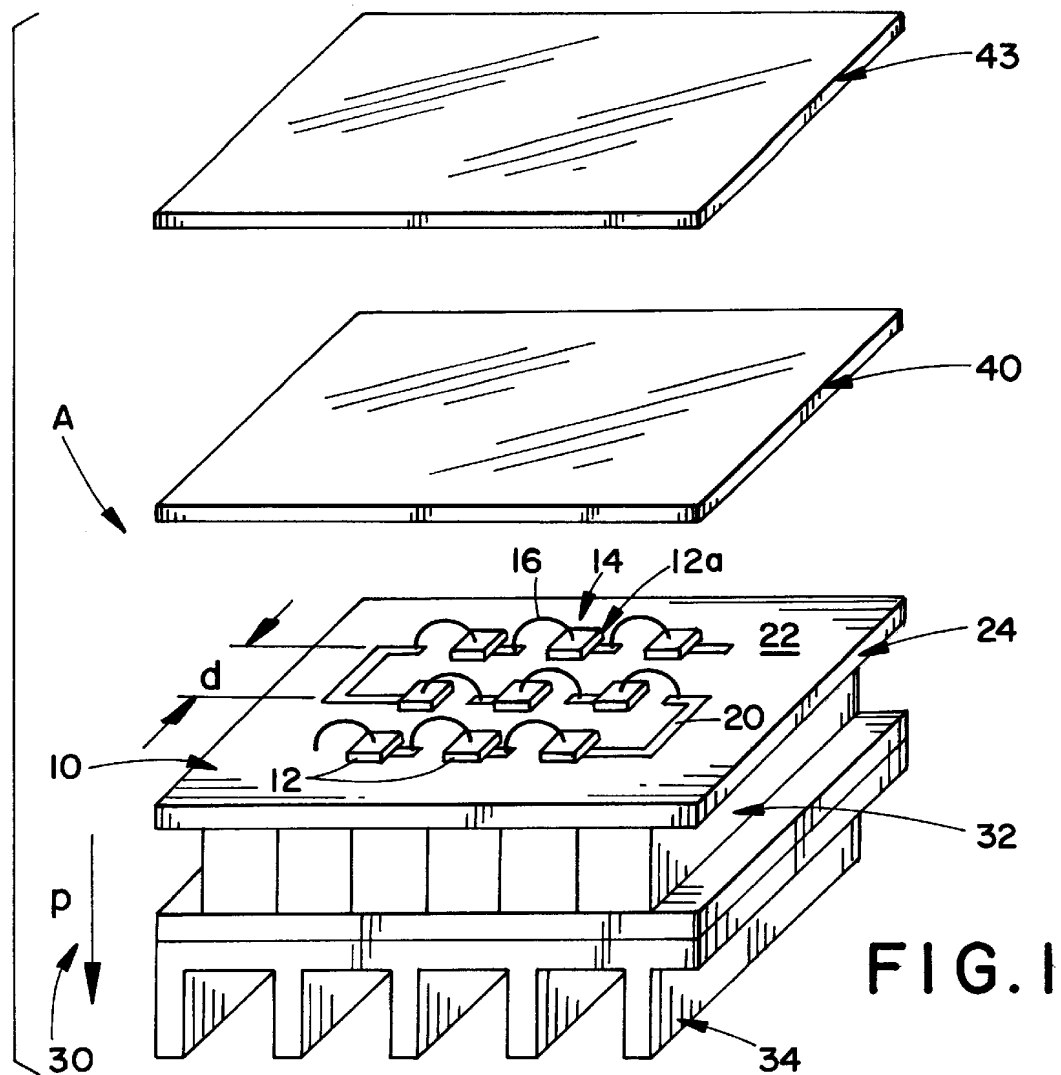
37 Claims, 4 Drawing Sheets

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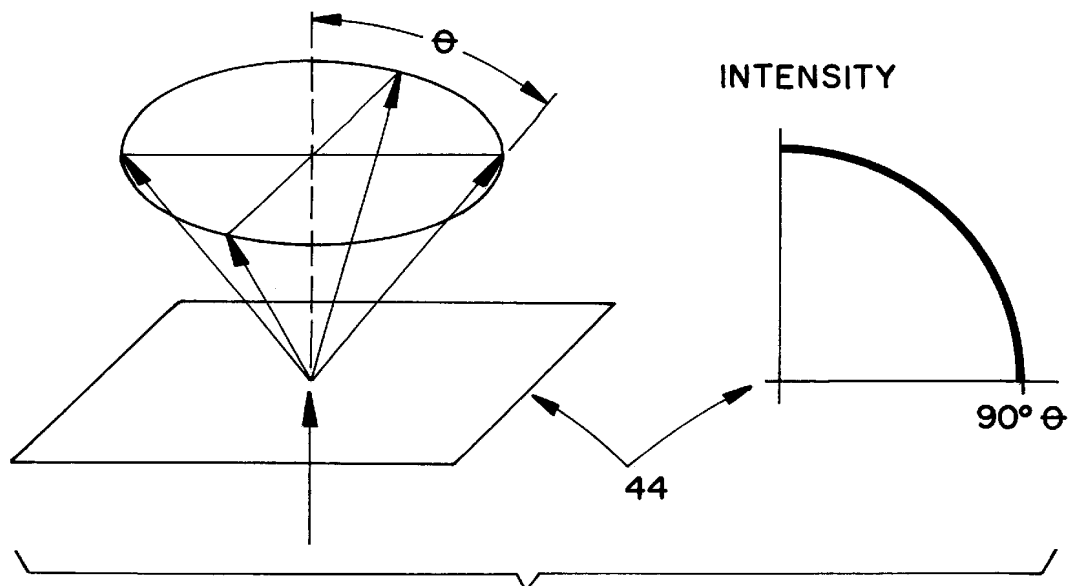


FIG. 3

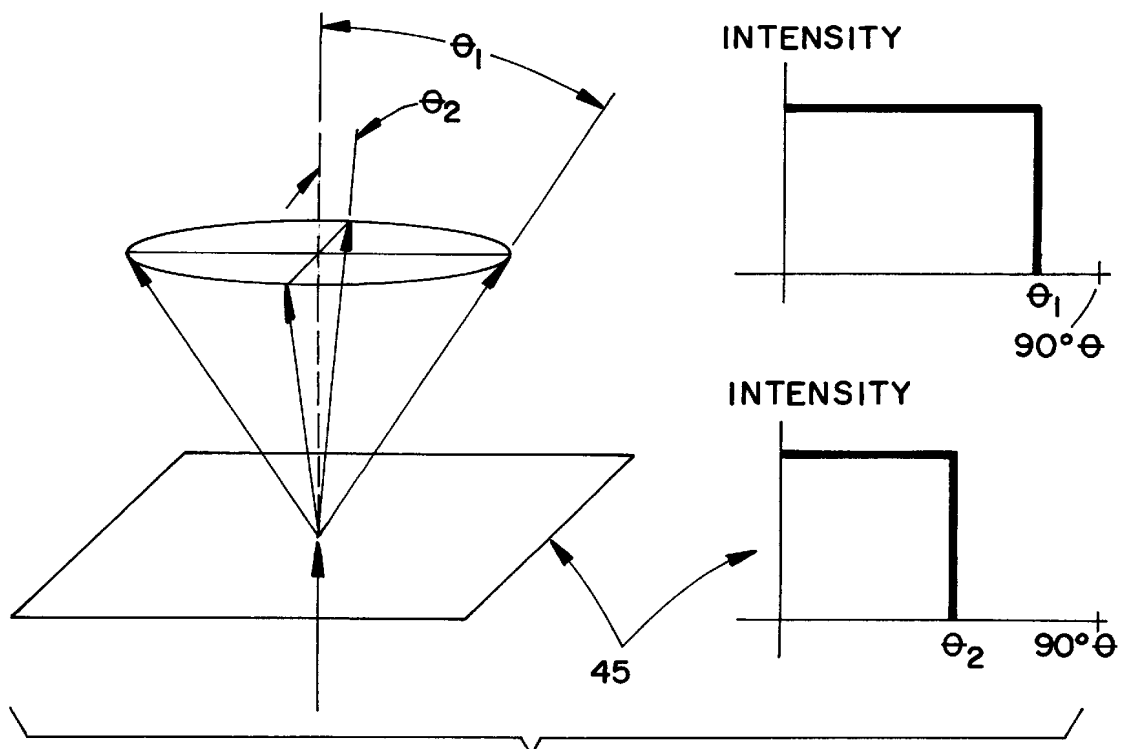


FIG. 4

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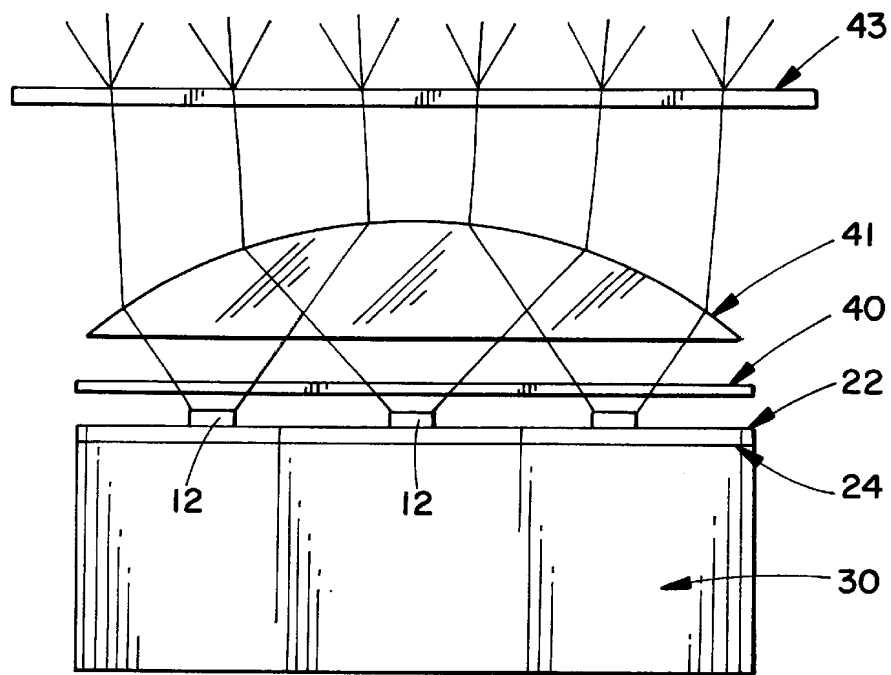


FIG. 5

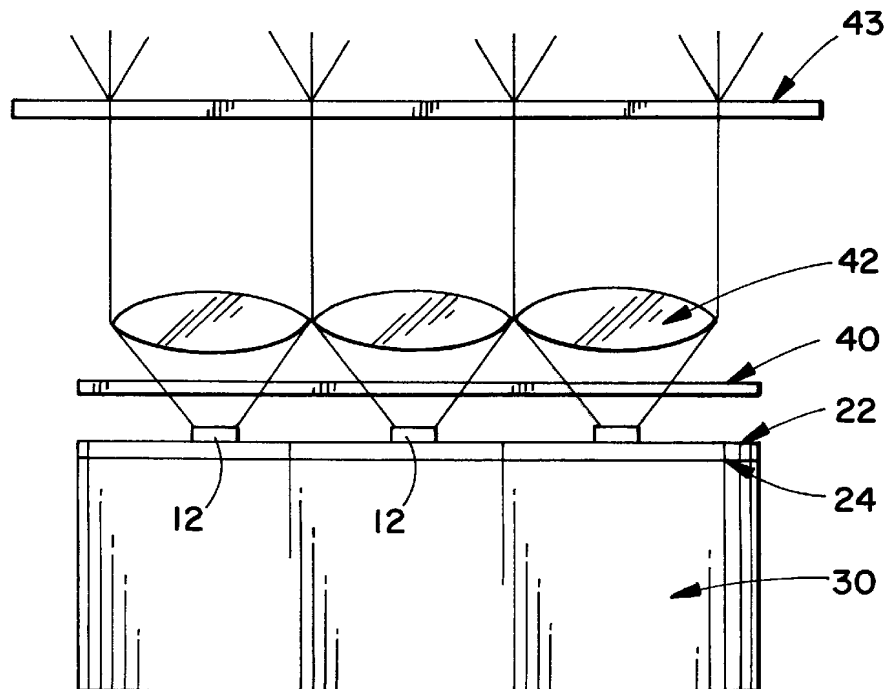


FIG. 6

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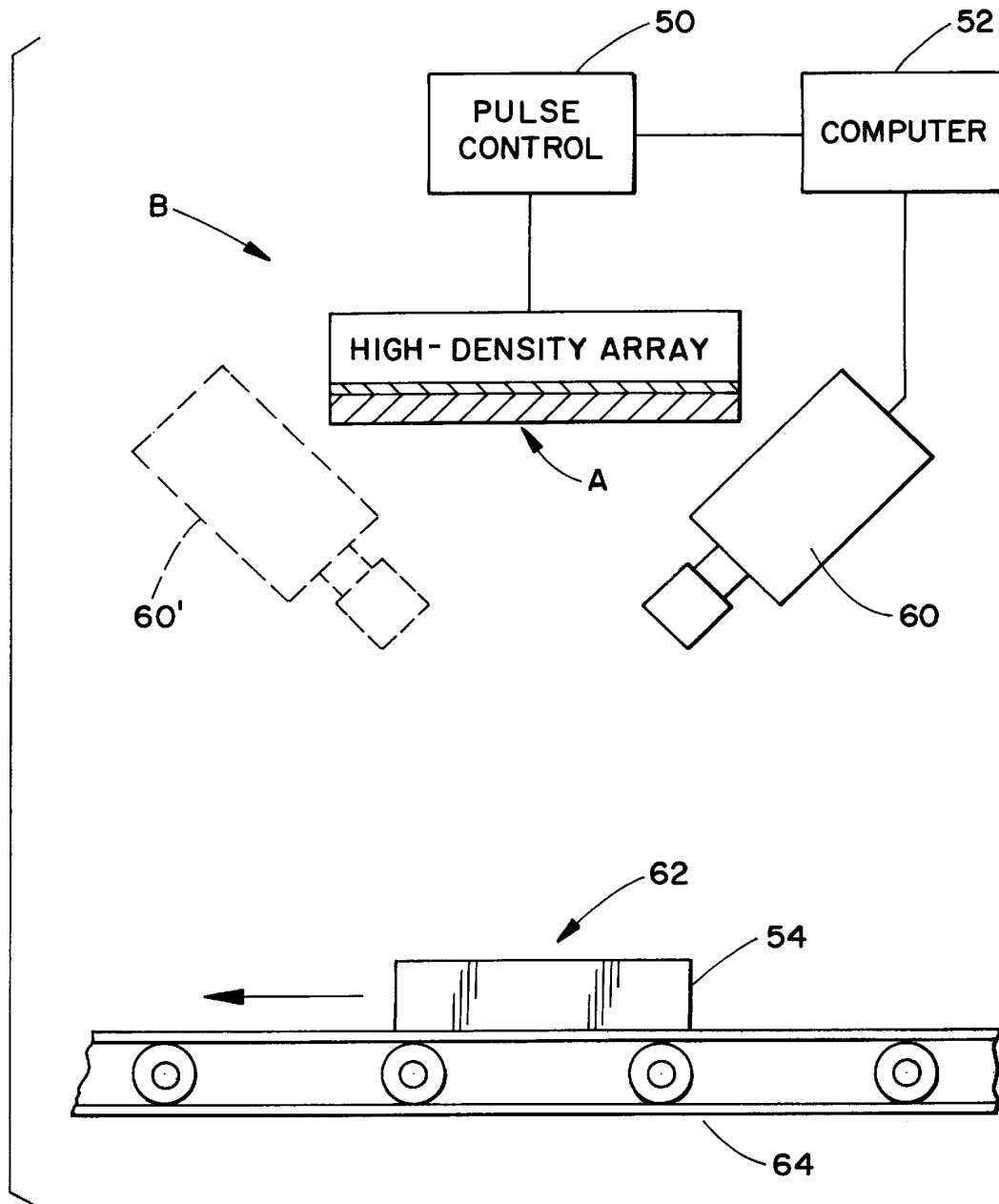


FIG. 7

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HIGH-DENSITY SOLID-STATE LIGHTING ARRAY FOR MACHINE VISION APPLICATIONS

BACKGROUND OF THE INVENTION

This application pertains to the art of illumination systems used in connection with automated visual inspection systems and will be described with reference thereto. However, it will be appreciated that the invention has broader applications, such as in the provision of an extremely reliable and uniform lighting system for any application requiring controlled illumination.

Machine vision continues to obtain increasing significance in industry to aid in robotic assembly systems as well as inspection systems for product sorting or quality control. Such machine vision systems are comprised generally of a lighting system to illuminate a specimen and a camera for capturing light reflected therefrom. A digitized image is formed from the light received by the camera.

More recently, implementations of configurable, solid-state lighting arrays and machine vision systems have improved significantly overall performance levels and quality in such systems. See, for example, U.S. Pat. No. 4,882, 498 to Cochran et al., commonly owned by the assignee hereof and incorporated herein by reference.

While initial techniques for forming solid-state lighting arrays provided significant improvement over earlier lighting systems, they nonetheless provided some limitations in obtainable total light output intensity, as well as being expensive to fabricate. These concerns are particularly significant in applications employing large lighting arrays, such as required for inspecting materials provided in a continuous web format, such as textiles, films, paper, metals, and the like.

Configurable solid-state lighting arrays are presently fabricated using individually packaged LED components. In such a construction, an individual light emitting p-n junction chip is typically encapsulated in a transparent epoxy. The epoxy acts to mechanically support the sensitive diode. Additionally, the epoxy capsulation is often molded into a spherical shape, thus giving it some lensing action. The lens-like characteristics of the epoxy encapsulation effectively concentrates the broad angular distribution of light emitted by a diode junction into a limited cone angle.

Such LED construction is often useful in applications in which the device is used as a panel or circuit board indicator. However, in machine vision applications wherein it is desirable to generate a uniform illumination pattern over a broad spatial field, the tendency of a lensed LED to generate illumination "hot spots" is deleterious.

Earlier attempts to address the hot spot problem have employed such means as diffusers disposed between LEDs and a target, or with an increase of a distance between the LED light source and the target.

Yet another draw back inherent to conventionally fabricated solid-state lighting arrays is the relatively large physical space requirement for epoxy packaging. A typical light emitting surface of a p-n junction is approximately 0.010 inches square. This small junction is usually encapsulated in a package with a diameter ranging from 0.10 inches to 0.25 inches. Thus, the ability to pack individual LEDs together into an array is constrained to a large degree by the packaging of the individual LED devices themselves.

Yet another disadvantage of illumination sources employing individually packaged LEDs is provided by virtue of the

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fact that the epoxy material in which they are encapsulated is a poor heat conductor. An important factor which limits the amount of light which may be emitted from an LED is the surface temperature of the associated emitting p-n junction. As surface temperature increases, the current-to-light-conversion efficiency of the device decreases correspondingly. Additionally, as the drive current of a device is increased, the power dissipated by the LED in the form of heat also increases. This tends to raise the surface temperature of the p-n junction. Thus, conventional LEDs are self-limited in the amount of light which they can generate.

The subject invention overcomes the above problems, and others, providing a dense array of solid-state light emitting diodes capable of providing an extremely high light output.

THE SUMMARY OF THE INVENTION

The present invention contemplates a new and improved machine vision inspection illumination system which overcomes all of the above-referred problems, and others, and provides solid-state illumination less expensively and with higher light output and improved lighting uniformity.

In accordance with the present invention, there is provided a high-density, solid-state lighting array which includes a dense array of semiconductor LEDs that are incorporated onto an electrically insulative, thermally conductive base portion. A heat dissipator is disposed in a thermally conductive path with the base portion so as to quickly communicate heat away from the LEDs.

In accordance with a more limited aspect of the present invention, the heat dissipating mechanism includes a thermal electric module which is suitably provided with a finned heat sink.

In accordance with another aspect of the present invention, the electrically insulative, thermally conductive base portion is comprised of at least one of beryllium oxide, aluminum oxide, and an insulated metal substrate.

In accordance with a yet more limited aspect of the present invention, a lens or window is provided between the lighting array and an associated specimen to direct and/or homogenize light resulting therefrom.

An advantage of the present invention is the provision of a solid-state lighting system which is particularly suited to automated machine vision systems.

Yet another advantage of the present invention is the provision of a solid-state illumination system which generates a high light output from a relatively inexpensive array.

Yet another advantage of the present invention is the provision of a solid-state illumination system which provides extremely uniform light output.

Further advantages will become apparent to one of ordinary skill in the art upon a reading and understanding of the subject specification.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may take physical form in certain parts, and arrangements of parts, a preferred embodiment of which is described in detail in the specifications and illustrated in the accompanying drawings which form a part hereof, and wherein:

FIG. 1 provides a perspective view of a solid-state illumination assembly in accordance with the present invention;

FIG. 2 shows an alternative embodiment of the array of the present invention;

FIG. 3 illustrates generally a Lambertian-type diffuser element;

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FIG. 4 illustrates generally a diffractive-type diffuser element;

FIG. 5 shows an alternative embodiment of the present invention;

FIG. 6 shows an alternative embodiment of the present invention; and,

FIG. 7 is a schematic diagram of a video inspection system employing the solid-state illumination array of the subject invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning now to the drawings wherein the figures are for the purpose of illustrating the preferred embodiment of the invention only, and not for the purpose of limiting the same, FIG. 1 illustrates a preferred embodiment of a high-density solid-state lighting array of the subject invention. The array A includes a base portion 10 comprised of an electrically-insulative, thermally-conductive material. Several high thermal conductivity substrates are advantageously used to form the base portion 10. Suitable materials include beryllium oxide (BeO), aluminum oxide (Al₂O₃), as well as insulated metal substrates (IMS) or graphite substrates. BeO and Al₂O₃ are ceramic compounds which provide good thermal conductivity combined with relatively poor electrical conductivity. Indeed, the substrate is selected for its ability to facilitate the conduction of locally generated thermal energy away from the lighting array while at the same time provide electric isolation to support parallel and series circuitry associated with the lighting array. IMS are composite materials which are comprised of a high thermal conductivity metal structure (such as copper, aluminum, or stainless steel) combined with a thin layer (about 0.003 inches thick) of ceramic film. Such ceramic film provides an electrically insulating layer upon which LED devices are secured, such as will be detailed below.

Typical thermal conductivity values for several of the substrate materials which are suitable for use in connection with the subject invention are presented below.

| MATERIAL | THERMAL CONDUCTIVITY (W/M · ° K.) |
|---------------------------------------|--------------------------------------|
| BeO | 220.3 |
| Al ₂ O ₃ | 29.8 |
| Copper | 398 |
| Aluminum | 205 |
| H ₂ O (reference) | .60 |
| FR-4 (standard printed circuit board) | .26 |

In the illustration of FIG. 1, the generally-planar base portion 10 has several lighting emitting elements in the form of light emitting diodes (LEDs) 12 disposed on a single surface thereof. The LEDs emit light when electrically forward biased. In the illustration, each of the LEDs 12 is formed of a semiconductor compound and has an associated p-n junction, a representative one of which is illustrated generally at 14. The selected semiconductor compound used to form the LEDs 12 has the property of directly converting a percentage of the electrons which are conducted through their volume into emitted photons in the UV, visible, and/or IR portions of the electromagnetic spectrum. The selected compound could comprise AlGaAs, AlInGaP, GaP, GaAs, and/or GaN. The p-n junction is disposed between a conductor such as 16 and each semi-conductor, a representative of which one of which is provided at 12a. A spacing d, which

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is approximately 0.05" (inches) in a preferred embodiment of the invention, is provided between rows of LEDs 12, which distance is chosen to maximize the optical output power of the LED array. The particular distance d is highly application specific and is contingent upon the particulars chosen for the fabrication of the array. Common power conductors, exemplarily shown at 20, are suitably disposed on the surface of the base portion 10 to provide electrical connections to each of the LEDs 12.

As noted above, all LEDs 12 are suitably fabricated on a single surface 22 of the base portion 10 in the lighting array or pattern. At high packing densities, such as the high density of the preferred embodiment (0.05" apart), management of the ancillary thermal energy generated during operation of the lighting array becomes one of the main issues governing the successful use of solid-state lighting arrays for general lighting applications. So, in the preferred embodiment, an opposite surface of the base portion 10, located at 24, is disposed adjacent to and in a thermally-conductive path to a heat dissipator, illustrated generally at 30, to reduce the temperature of the LEDs within the array. In the preferred embodiment, the heat dissipator 30 is an active heat reservoir capable of freely exchanging thermal energy with the ambient environment and includes a thermal-electric cooler 32 and a finned heat sink 34. Forced air is used to facilitate the thermal transfer of energy from the finned heat sink to the ambient environment.

FIG. 2 shows a structure representative of alternatives for the heat dissipator 30. For example, the heat reservoir could be a cavity-filled structure capable of supporting fluid flow which, in turn, facilitates thermal transfer of energy from the heat reservoir to the ambient environment. It will further be appreciated that various other active and passive cooling devices are suitably implemented as the heat dissipator 30. For example, re-circulated water, Carnot cycle coolers, Stirling cycle coolers, thermo-electric coolers, and refrigerated water chillers and other active cooling components are suitably implemented.

Referring again to FIG. 1, application of electric current to the thermal-electric module 32 provides for conduction of heat from the base unit 10, through its second surface 24, to the finned heat sink 34. Thus, substantial amounts of heat may be quickly conducted away from the LEDs 12, which are relatively densely packed. Operating in this fashion, the emitting diodes can potentially be driven to temperatures below the ambient air temperature. In the preferred embodiment, chip packing density is advantageously in the order of 400 LEDs per square inch.

Also illustrated in FIG. 1 is a thermal conductivity path p, which evidences flow of heat from the LEDs 12, through the thermal-electric cooler 32, to the finned heat sinks 34. The thermal conductivity path p is also shown in FIG. 2.

A translucent window 40 is advantageously disposed adjacent to the array. Three lensing options are contemplated, each of which is particularly advantageous for specified illumination applications.

In a first option, raw un-focussed radiation fields produced by LEDs 12 of the array are available for specified applications. That is, the optical radiation emitted by the device may be used in either transmission or reflection within systems performing online process control and/or machine vision inspection applications. Parameters such as intensity, illumination geometry, spectral content, angular distribution, and relative uniformity may be controlled to optimize the illumination for a particular machine vision inspection or process control application. Moreover, a dif-

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fuser element generally, representatively shown at **43** may be employed to direct the emitted radiation to a preselected area, as those skilled in the art will appreciate. For example, the diffuser element may be a Lambertian-type diffuser **44** (ground glass, etc.), as shown in FIG. **3**, or a diffractive-type diffuser **45**, as shown in FIG. **4**, capable of generating either circular or elliptical illumination patterns. FIGS. **3** and **4** also show graphs of intensity versus the angle θ to illustrate operational characteristics of the respective diffusers.

In a second option, as illustrated in FIG. **5**, a macro lens **41** is suitably used to manipulate the complete radiation field emitted by the array to direct the light as a whole to a preselected area. By way of example, a cylindrical lens can suitably be located over top of the entire array. Preferably, the macro lens utilizes one or more of refraction, reflection, and diffraction to induce desired lensing action. In addition, as with the first lensing option, a diffuser element generally shown at **43** may be used to direct emitted light to a preselected area. For example, the diffuser element may be a Lambertian-type diffuser **44** (ground glass, etc.) (FIG. **3**) or a diffractive-type diffuser **45** (FIG. **4**) capable of generating either circular or elliptical illumination patterns.

Referring now to FIG. **6**, a third lensing choice for use with the translucent window **40** is a plurality of lenses arranged as a lenslet array **42** to direct light generated by each of the LEDs **12** to a preselected area. The lensing action of such a lenslet array is suitably refractive, reflective, diffractive, or a combination of methods, the choice being highly application specific to induce a desired lensing action. Various lenslet arrays are well known in the art and available in the marketplace. Again, a diffuser element generally shown at **43** may be used to direct light to a preselected area. For example, such a diffuser element may be a Lambertian-type diffuser **44** (ground glass, etc.) (FIG. **3**) or a diffractive-type diffuser **45** (FIG. **4**) capable of generating either circular or elliptical illumination patterns.

It will be appreciated that various wiring schemes, such as parallel or serial configurations, may be utilized among the LEDs **12**. This provides for a high degree of selective configureability of the LED array during the design process.

Turning now to FIG. **7**, an example inspection system B employing the high-density solid-state lighting array A of FIG. **1** is provided. The system B includes a lighting control unit **50** which provides selected drive current and/or pulse duration and rate parameters to the array A.

In a pulsed-current mode, such as that advantageously used for freezing images, pulse duration and period and pulse current are electronically configurable. The lighting control unit **50** provides pulsed current to LEDs of the array A. A suitable range of such pulsed current is 0.1 amp up to 10 amps. The lighting control unit **50** also controls the pulse duration and duty cycle, or period, of array A. Pulse durations are suitably in the range of 1 to 1000 μ sec. In addition, a suitable duty cycle or ratio of off-time to on-time is in the range of 2:1 to 1000:1, with 300:1 being a typical operation condition. In addition, different geometric areas within the array may be independently addressable as a function of current level and pulse duration. In one embodiment, the LEDs all emit optical radiation of essentially the same limited wavelength range so that the control unit **50** provides a configurable intensity and geometry functionality which can be utilized to optimize the emitted radiation fields for a given application area. In a second embodiment, LEDs of two or more emission wavelengths are disposed in the array such that the control unit **50** will provide to the array a configurable intensity, geometry, and spectral content func-

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tionality to be utilized to optimize the emitted radiation fields for a given application area.

In a continuous mode, the drive current to the LEDs is an electronically configurable parameter and the lighting control unit **50** provides controlled continuous current to the individual LED's in the range of 1 to 200 mA. In addition, different geometric areas within the array may be independently addressable as a function of current level. In one embodiment, the LEDs all emit optical radiation of essentially the same limited wavelength range so that the control unit **50** provides a configurable intensity and geometry functionality which can be utilized to optimize the emitted radiation fields for a given application area.

The lighting control unit **50** operates under the direction and control of a suitable computer system **52**. A camera or image acquisition means is illustrated generally at **60**. It will be appreciated, however, that additional cameras, such as that **60'**, are also suitably utilized. Camera or cameras **60** are trained onto an inspection area **62** which is selectively illuminated by the array A under control of the lighting control unit **50** and the computer **52**. Images of a specimen **54** disposed in the illumination area **62** are acquired by the camera or cameras. Such images are communicated to the computer system **52** for analysis. From the illustration, it will be appreciated that a series of specimens **24** may be selectively or serially communicated to the viewing area **62** by moving them along a conveyor **64**, or the like.

This invention has been described with reference to the preferred and alternate embodiments. Obviously, modifications and alterations will occur to others upon the reading and understanding of the specification. It is intended that all such modifications and alterations be included insofar as they come within the scope of the appended claims or the equivalents thereof.

Having thus described the invention, we now claim:

1. A machine vision apparatus comprising:
 - a lighting array for selectively illuminating a viewing area comprising,
 - a plurality of individual light emitting elements formed of a semiconductor compound which directly converts a percentage of electrons which are conducted through their volume into emitted photons in one of UV, visible, and/or IR portions of an electromagnetic spectrum, the light emitting elements being placed within a one- or two-dimensional pattern wherein element spacing is less than or equal to 0.05",
 - an electrically insulative, thermally conductive support substrate having a thermal conductivity greater than 1 W/m $^{\circ}$ K upon which the light emitting elements are directly attached in formation of the pattern, said support substrate specifically selected for its ability to facilitate conduction of locally generated thermal energy away from the light emitting elements while at the same time providing a sufficient degree of electrical isolation required to support parallel and series circuit construction associated with the individual light-emitting elements, and,
 - a heat dissipater disposed in direct thermal contact with the thermally conductive support substrate reducing the temperature of the light-emitting elements within the array;
 - a camera for acquiring images of specimens disposed in the illuminated viewing area;
 - a lighting control unit in communication with the lighting array; and,
 - a computer in communication with the camera to receive the acquired images and in communication with the lighting control unit.

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2. The apparatus of claim 1 wherein the electrically insulative, thermally conductive substrate is comprised of at least one of beryllium oxide (BeO), alumina (Al₂O₃), insulated metal substrate and graphite substrate.

3. The apparatus of claim 1 wherein the semiconductor compound is comprised of one or more of the following chemical compounds: AlGaAs, AlInGaP, GaP, GaAs, and GaN.

4. The apparatus of claim 1 wherein the heat dissipator is comprised of at least one of a Carnot-cycle cooler, a Stirling-cycle cooler, thermo-electric cooler, and a refrigerated water chiller.

5. The apparatus of claim 1 wherein the heat dissipator is an active heat reservoir freely exchanging thermal energy with ambient environment of the lighting array.

6. The apparatus of claim 5 wherein the heat reservoir is a finned heat sink.

7. The apparatus of claim 6 wherein forced air is used to facilitate thermal transfer of energy from the finned heat sink to the ambient environment.

8. The apparatus of claim 5 wherein the heat reservoir is a cavity-filled structure capable of supporting fluid flow which, in turn, facilitates thermal transfer of energy from the heat reservoir to the ambient environment.

9. An apparatus comprising:

a lighting array for selectively illuminating a viewing area comprising,

a plurality of individual light emitting elements formed of a semiconductor compound which directly converts a percentage of electrons which are conducted through their volume into emitted photons in one of UV, visible, and IR portions of an electromagnetic spectrum, the light emitting elements being placed within a one- or two-dimensional pattern wherein element spacing is less than or equal to 0.05",

an electrically insulative, thermally conductive support substrate upon which the light emitting elements are attached in formation of the pattern, said support substrate specifically selected for its ability to facilitate conduction of locally generated thermal energy away from the light emitting elements while at the same time providing a sufficient degree of electrical isolation required to support parallel and series circuit construction associated with the individual light-emitting elements, and,

a heat dissipater disposed in direct thermal contact with the thermally conductive support substrate reducing the temperature of the light-emitting elements within the array;

a camera for acquiring images of specimens disposed in the illuminated viewing area;

a lighting control unit in communication with the lighting array; and,

a computer in communication with the camera to receive the acquired images and in communication with the lighting control unit.

10. The apparatus of claim 9 wherein optical radiation fields emitted by the plurality of individual light emitting elements are used, in either transmission and/or reflection, within systems performing on-line process control and/or machine vision inspection applications.

11. The apparatus of claim 10 wherein at least one of intensity, illumination geometry, spectral content, angular distribution and relative uniformity associated with the emitted optical radiation fields are controlled in order to optimize the resultant illumination for a selected machine vision inspection or process control application.

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12. The apparatus of claim 11 further comprising a macro lens to direct light generated by the plurality of individual light emitting elements as a whole to a preselected area.

13. The apparatus of claim 12 wherein the macro lens utilizes at least one of refraction, reflection, and diffraction to induce desired lensing action.

14. The apparatus of claim 12 further comprising a diffuser element to direct light emitted by the plurality of individual light emitting elements to a preselected area.

15. The apparatus of claim 14 wherein the diffuser element is a Lambertian-type diffuser.

16. The apparatus of claim 14 if wherein the diffuser element is a diffractive-type diffuser generating either circular or elliptical illumination patterns.

17. The apparatus of claim 11 further comprising a plurality of lenses arranged as a lenslet array to direct light generated by the plurality of individual light emitting elements to a preselected area.

18. The apparatus of claim 17 wherein individual elements of the lenslet array utilize at least one of refraction, reflection, and diffraction to induce the desired lensing action.

19. The apparatus of claim 17 further comprising a diffuser element to direct light emitted by the plurality of individual light emitting elements to a preselected area.

20. The apparatus of claim 19 wherein the diffuser element is a Lambertian-type diffuser.

21. The apparatus of claim 19 wherein the diffuser element is a diffractive-type diffuser generating either circular or elliptical illumination patterns.

22. The apparatus of claim 11 further comprising a diffuser element to direct light emitted by the plurality of individual light emitting elements to a preselected area.

23. The apparatus of claim 22 wherein the diffuser element is a Lambertian-type diffuser.

24. The apparatus of claim 22 wherein the diffuser element is a diffractive-type diffuser generating either circular or elliptical illumination patterns.

25. The apparatus of claim 11 wherein at least one of pulse duration and period and drive current associated with the array are electronically configurable to optimize the emitted optical radiation fields for a selected application.

26. The apparatus of claim 25 wherein the plurality of individual light emitting elements are operated in a pulsed-current mode.

27. The apparatus of claim 26 wherein the pulse duration and period are electronically configurable parameters.

28. The apparatus of claim 26 wherein the drive current to the lighting elements is an electronically configurable parameter.

29. The apparatus of claim 26 further comprising varying geometric areas within the array which are independently addressable as a function of the drive current and the pulse duration.

30. The apparatus of claim 29 wherein each of the plurality of light emitting elements emit optical radiation of essentially the same limited wavelength range so that an electronic control unit provides the array with a configurable intensity and geometry capability to optimize the emitted radiation fields for a selected application area.

31. The apparatus of claim 29 wherein elements of the plurality of individual light emitting elements of two or more emission wavelengths are contained within the array so that an electronic control unit provides the array with a configurable intensity, geometry, and spectral content capability to optimize the emitted radiation fields for a selected application area.

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32. The apparatus of claim 25 wherein the plurality of individual light emitting elements are operated in a continuous-current mode.

33. The apparatus of claim 32 wherein the drive current to the plurality of individual light emitting elements is an electronically configurable parameter. 5

34. The apparatus of claim 32 further comprising varying geometrical areas within the array which are independently addressable as a function of the drive current.

35. The apparatus of claim 34, wherein each of the individual light emitting elements emit optical radiation of essentially the same limited wavelength range so that an electronic control unit provides the array with a configurable intensity and geometry capability to optimize the emitted radiation fields for a selected application area. 10

36. The apparatus of claim 34 wherein elements of the plurality of light emitting elements of two or more emission wavelengths are contained within the array so that an electronic control unit provides the array with a configurable intensity, geometry, and spectral content capability to optimize the emitted radiation fields for a selected application area. 15 20

37. A method of performing machine vision and/or process control operations, the method comprising steps of:

providing a camera to be positioned to view specimens in a viewing area; 25

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providing a plurality of individual light emitting elements formed of a semiconductor compound which directly converts a percentage of electrons which are conducted through their volume into emitted photons in one of UV, visible, and IR portions of an electromagnetic spectrum;

arranging the plurality of light emitting elements in a pattern wherein element spacing is less than or equal to 0.05" on an electronically insulative, thermally conductive support substrate;

implementing the arranged array as a light source;

illuminating the viewing area with the arranged array;

conducting locally generated thermal energy away from the light emitting elements by the support substrate to a heat dissipater disposed in direct thermal contact with the thermally conductive support substrate for reducing the temperature of the light-emitting elements within the array;

acquiring images of the specimens in the viewing area by the camera; and

transmitting the acquired images to a computer.

* * * * *

EXHIBIT U-4



US005278432A

United States Patent [19]

Ignatius et al.

[11] **Patent Number:** 5,278,432[45] **Date of Patent:** Jan. 11, 1994[54] **APPARATUS FOR PROVIDING RADIANT ENERGY**[75] Inventors: **Ronald W. Ignatius; Todd S. Martin**, both of Dodgeville, Wis.[73] Assignee: **Quantam Devices, Inc.**, Barneveld, Wis.[21] Appl. No.: **936,570**[22] Filed: **Aug. 27, 1992**[51] Int. Cl.⁵ **H01L 33/00**[52] U.S. Cl. **257/88; 257/99; 257/723; 362/800; 307/311**[58] **Field of Search** **257/88, 98, 99, 723, 257/706, 918; 313/500, 512; 362/800; 307/311; 47/DIG.**[56] **References Cited****U.S. PATENT DOCUMENTS**

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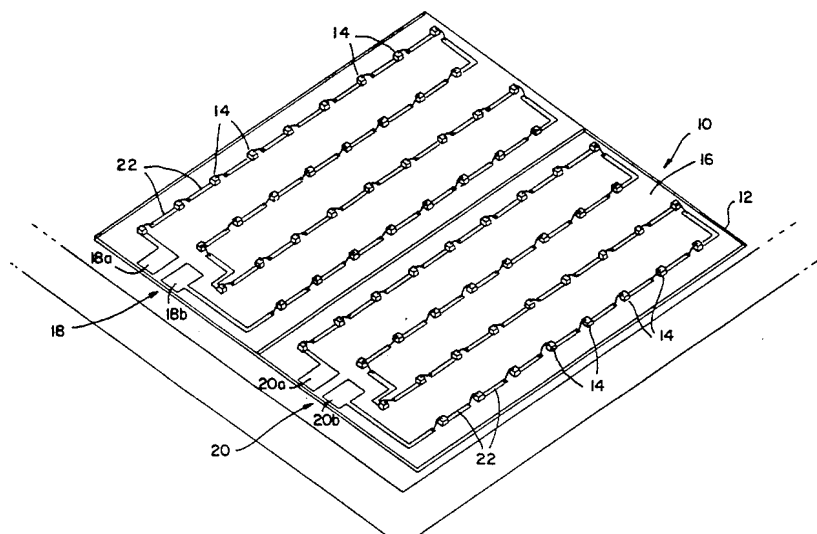
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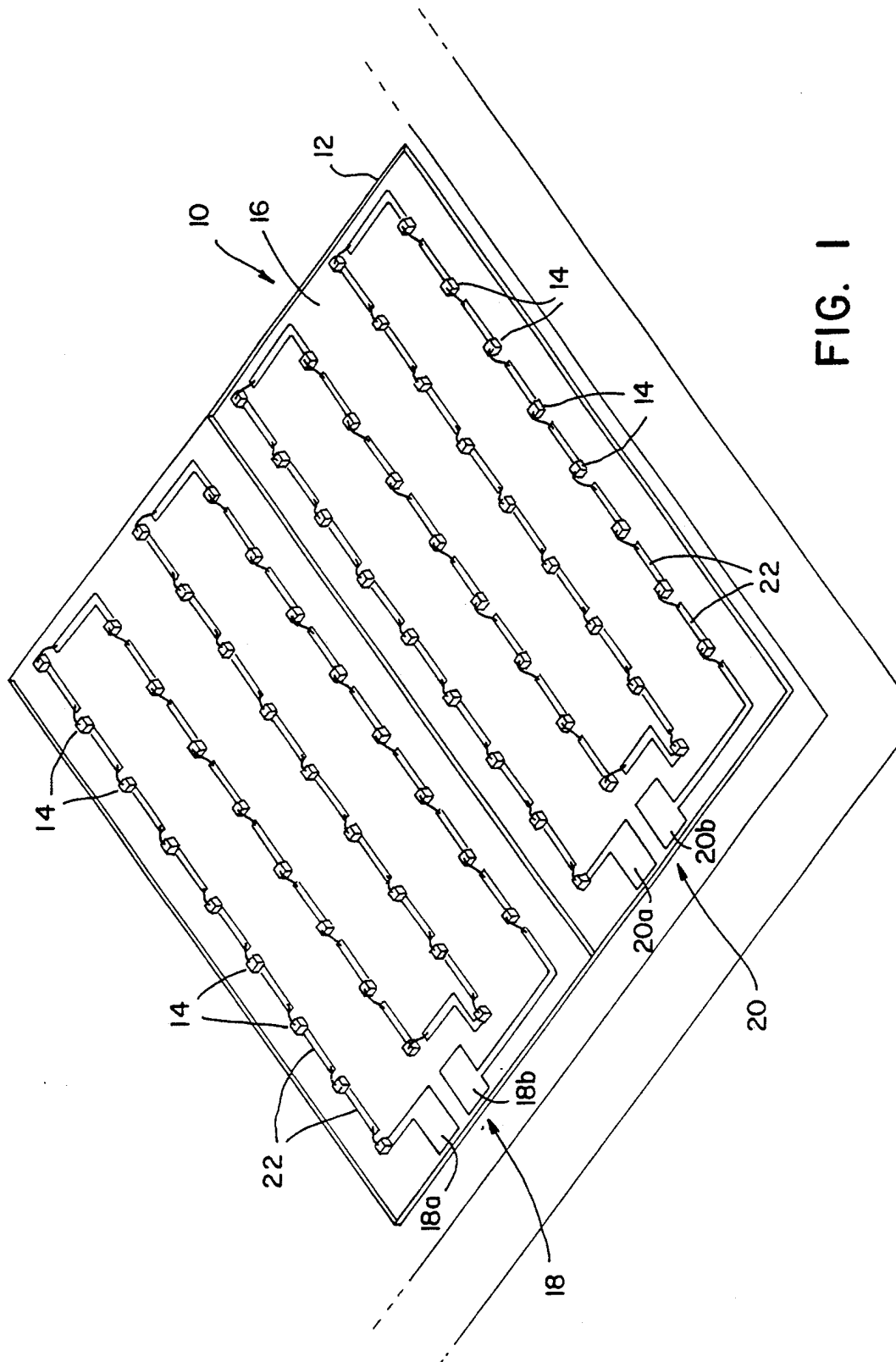
Primary Examiner—William Mintel*Assistant Examiner*—Minhloan Tran*Attorney, Agent, or Firm*—Andrus, Scales, Starke & Sawall

[57]

ABSTRACT

The monolithic hybrid LED array includes a metal heat sink substrate, a ceramic layer on the substrate, and a plurality of series-connected epitaxially-formed LEDs connected by interconnects such as conductive ink strips. The array preferably includes three to six sets of series-connected LEDs that are tightly packed on the substrate. The LEDs are housed in a modular housing having a power regulating circuit and an override feature for overriding the regulator to produce the maximum LED output for brief periods of time. The regulator may continuously vary the light intensity output from the equivalent of 0 to 2000 micromols per second per meter squared.

33 Claims, 5 Drawing Sheets



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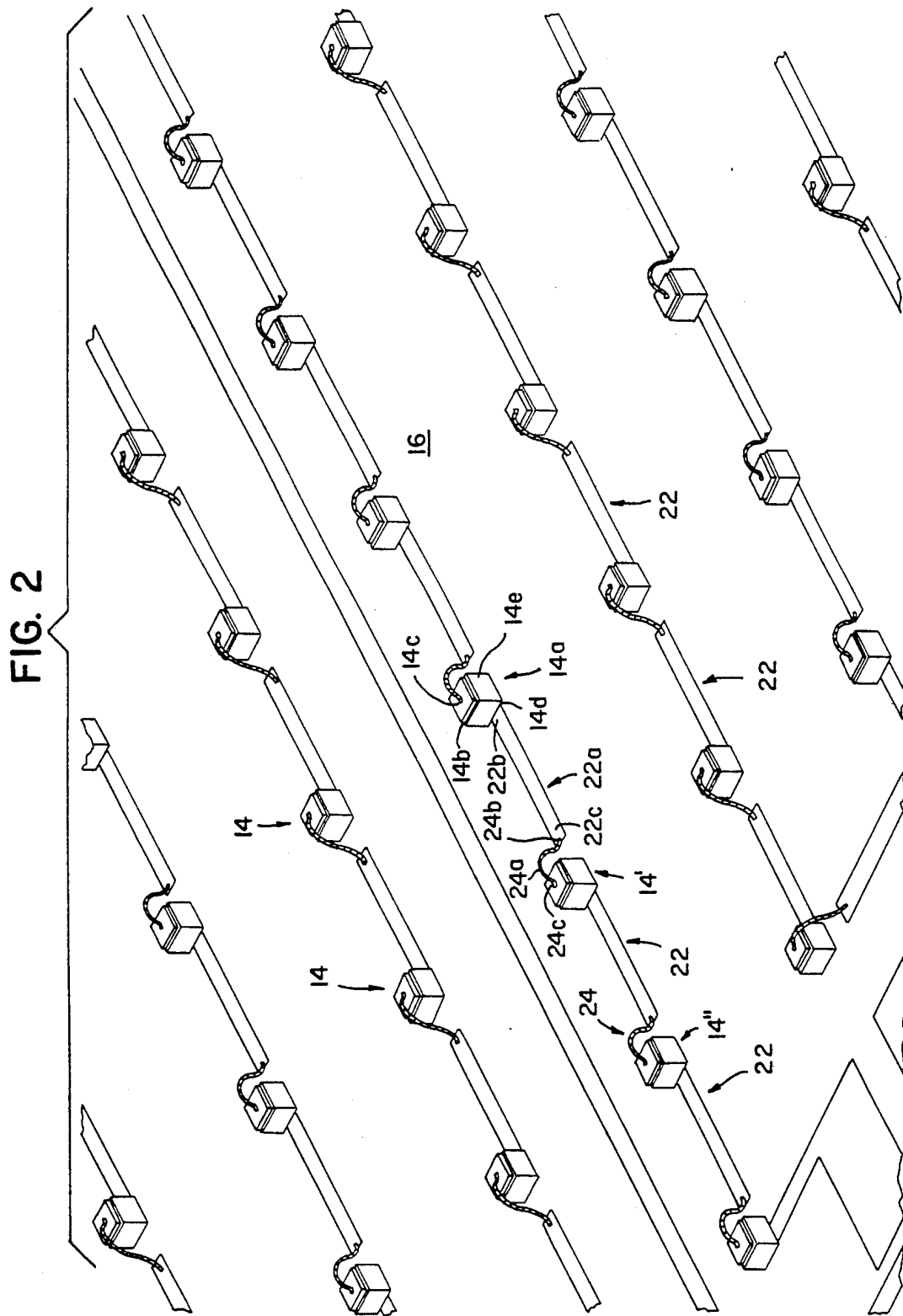


FIG. 3

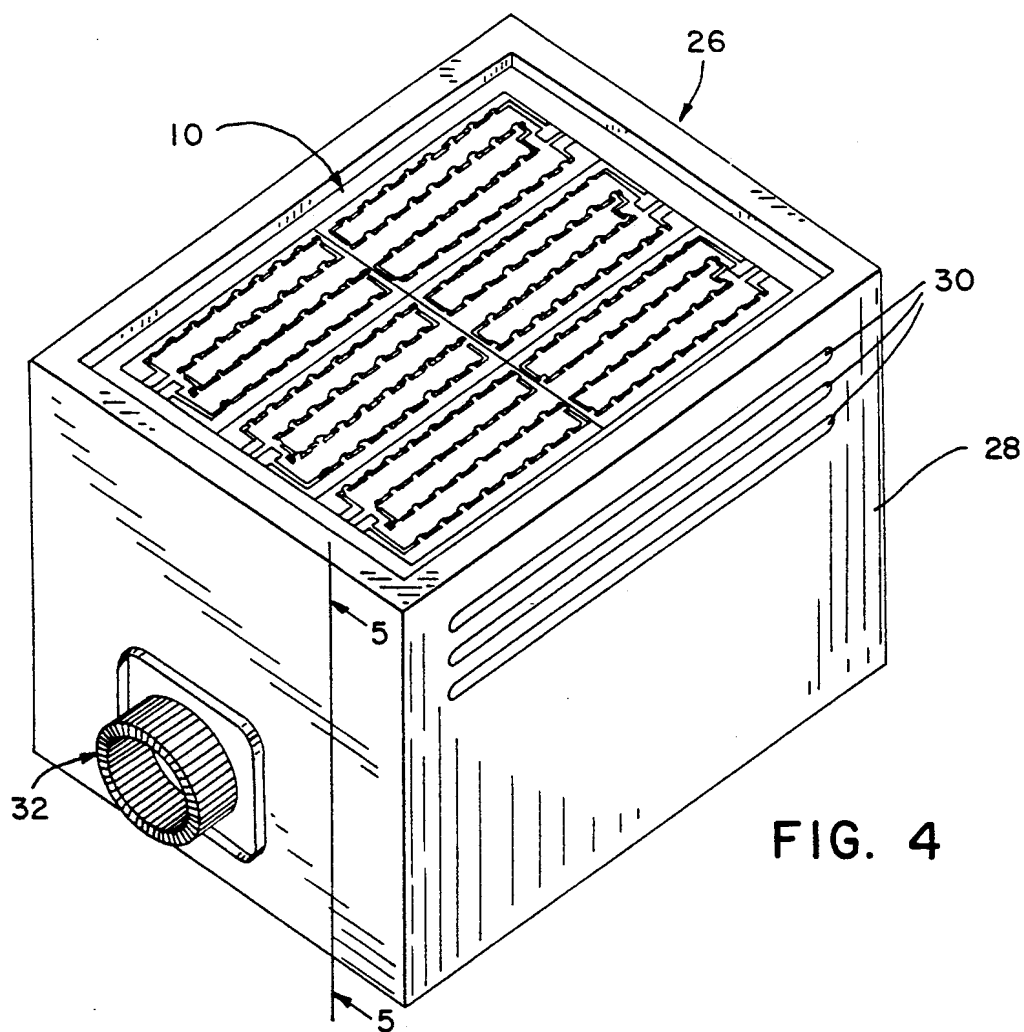
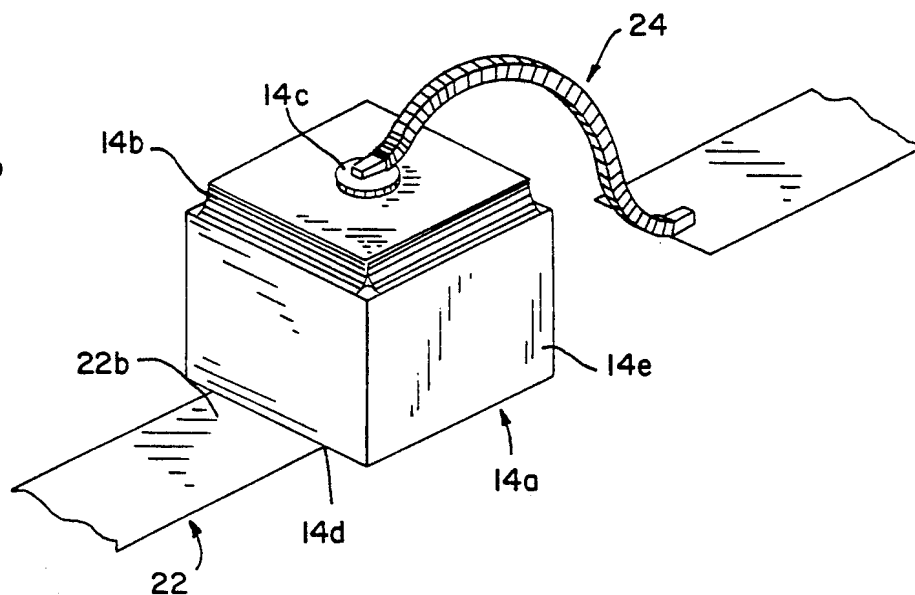


FIG. 4

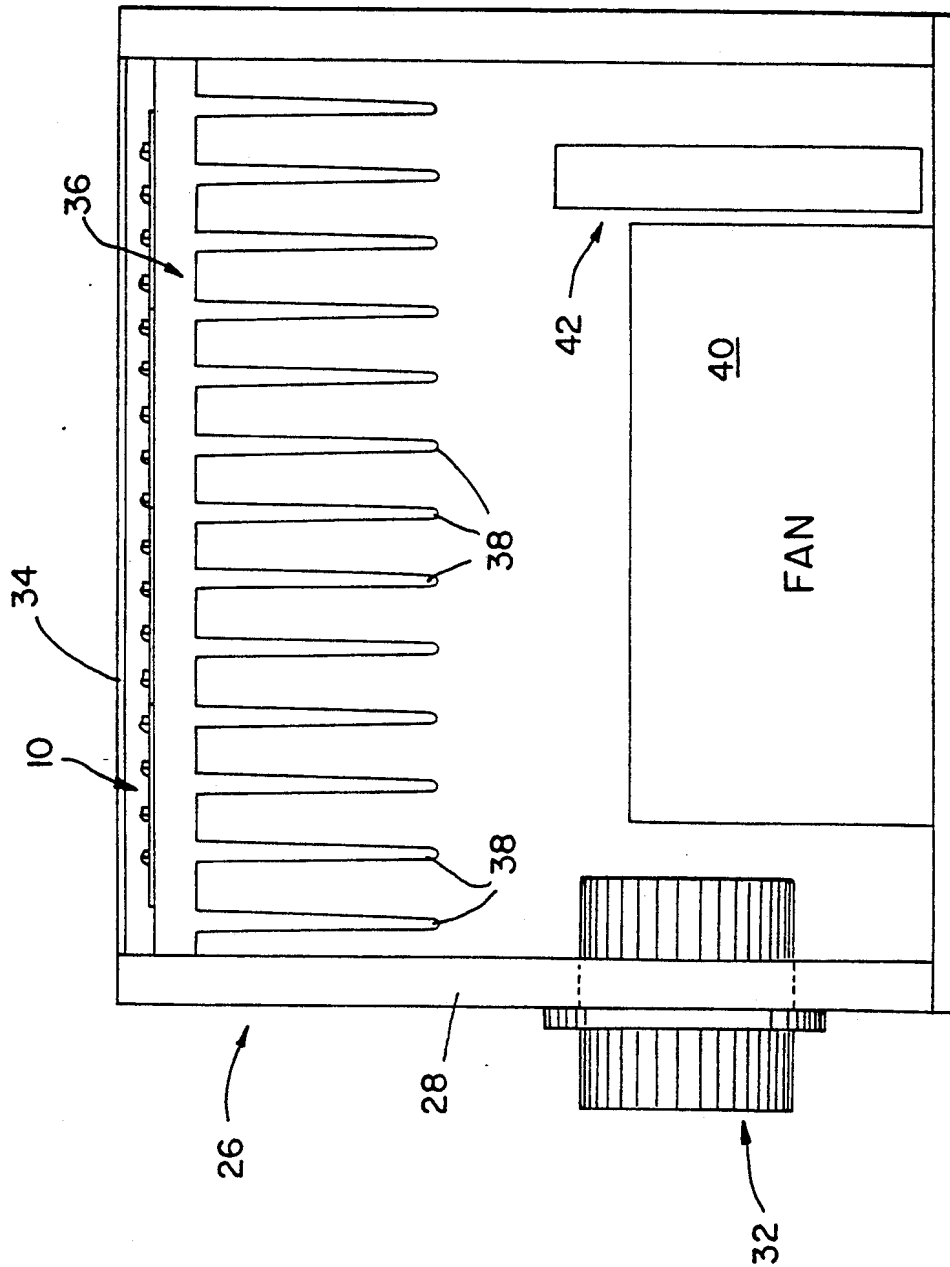
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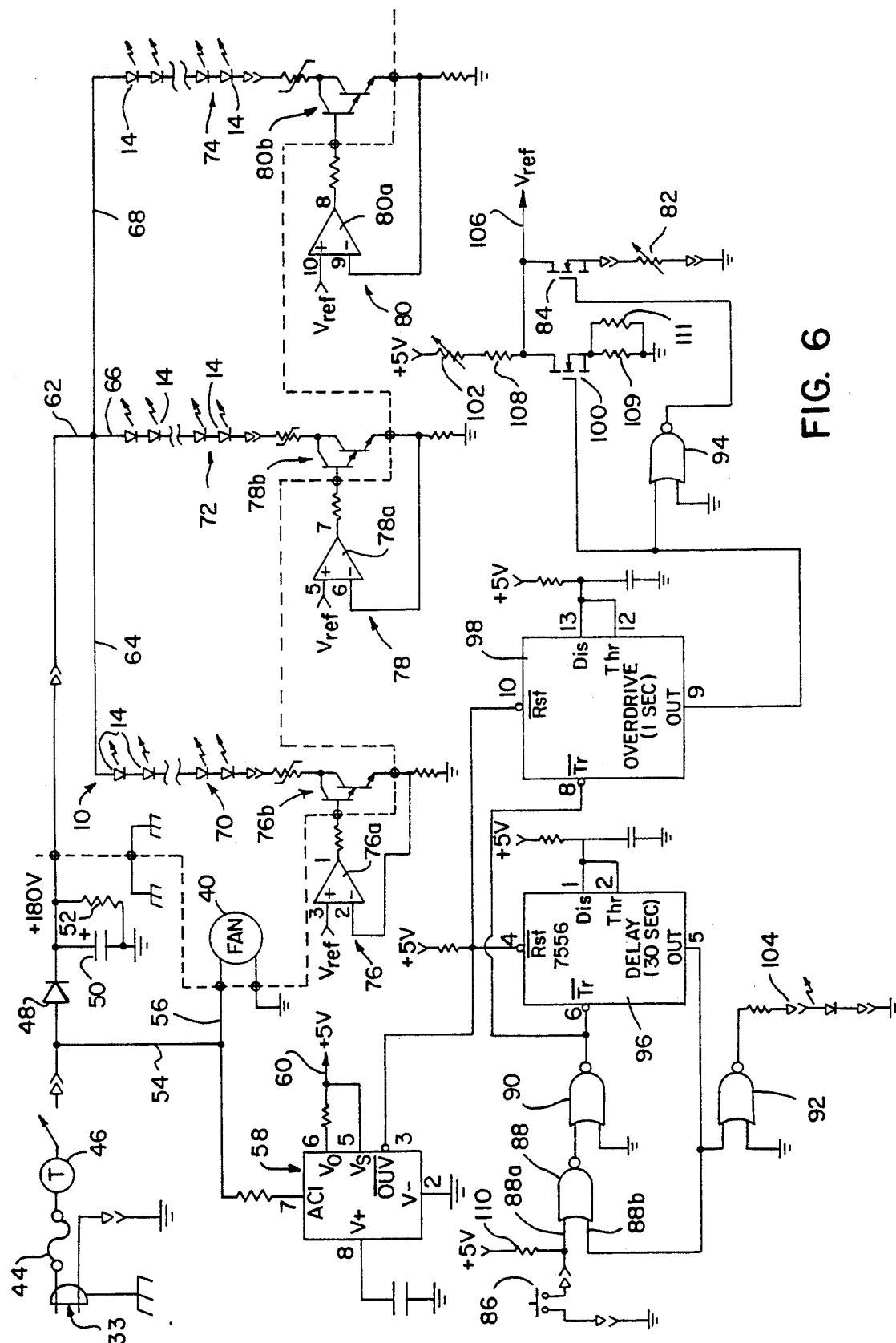
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FIG. 5





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APPARATUS FOR PROVIDING RADIANT ENERGY

BACKGROUND OF THE INVENTION

This invention relates to apparatus for providing radiant energy to enhance and test plant growth, and more particularly to apparatus that uses optoelectronic devices such as light emitting diodes to provide such radiant energy.

Several types of devices are known for providing radiant energy to enhance and test plant growth. Typical prior art electrical light sources include fluorescent, high pressure sodium, and other metal halide lamps. These prior art devices have several major disadvantages.

One disadvantage of metal halide lamps is that they provide a great deal of infrared and/or heat energy. Excessive infrared and heat energy has a deleterious effect on plants. To overcome this disadvantage, typical prior art devices must be placed at a sufficient distance from the plant to prevent plant damage. When the device is being used with a leaf chamber to test the ability of the plant to transform the radiant energy into chemical energy, extensive additional apparatus is required to remove the infrared and heat energy to prevent harm to the leaf. The use of such additional cooling and ventilating apparatus greatly increases the effective cost of the radiant energy.

Another disadvantage of metal halide energy sources is that the light intensity cannot be continuously reduced to a zero intensity since metal halide lamps require a minimum voltage to maintain the arc in the lamp. Since it is often desirable to reduce the energy output to a zero or a near zero intensity, the metal halide lamps are not suitable for some applications.

Typical prior art metal halide and other electrical energy sources output light having a relatively broad spectrum. However, it has been found that plant growth does not require the full spectrum of visible light. Thus, it is desirable to provide radiant energy sources that emit radiation in one or more specific regions of the spectrum.

U.S. Pat. No. 5,012,609 issued May 7, 1991 to Ignatius et al discloses an array of light emitting diodes which provide radiant energy in specific regions of the spectrum. However, a light emitting diode array like that disclosed in U.S. Pat. No. 5,012,609 requires a plurality of discrete light emitting diodes that must be plugged into a circuit. That arrangement limits the number of light emitting diodes that may be packed into the array. It is also somewhat expensive to manufacture and assemble an array of light emitting diodes using discrete components. Also, the power requirements for such arrays, as well as for metal halide lamps, are relatively large, increasing the cost of operation of the electrical energy sources.

SUMMARY OF THE INVENTION

A unique hybrid monolithic array of opto-electronic devices such as light emitting diodes or cold cathode fluorescent devices is disclosed that may be used to enhance and test plant growth as well as to irradiate samples of other types of living cells.

In a preferred embodiment, the array includes a thermally conductive substrate made of aluminum or copper that acts as a heat sink. Disposed on top of the substrate is a substantially non-electrically conductive ce-

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ramic layer. A plurality of epitaxially-formed, double heterojunction, double power light emitting diodes (LEDs) are bonded to the ceramic layer. The LEDs are preferably formed of a gallium aluminum arsenide material so that they emit substantially monochromatic light having 620-680 and/or 700-760 nm wavelengths that are particularly desirable for plant growth. The array may also include silicon carbide LEDs that emit substantially monochromatic light have a 400-500 nm wavelength.

The array may contain multiple sets of series-connected LEDs. In each set of LEDs, adjacent LEDs are electrically connected by interconnects such as conductive strips deposited on the ceramic layer. The interconnects are preferably made from a metal-containing ink, although they could consist of a metal lead frame or wires. The array is arranged such that a first electrode of a first LED is electrically connected to one end of the interconnect. The opposite end of the interconnect is electrically connected to an opposite polarity electrode of an adjacent, series-connected LED, preferably by a standard wire. The body of each LED, including its heterojunctions, is preferably substantially encased in a passivation material, and is bonded to the ceramic layer using an electrically-conductive epoxy adhesive. The entire array is coated with a conformal coating of a transparent epoxy material to protect it during handling.

In a preferred embodiment, each set of series-connected LEDs includes 34 LEDs disposed on a one inch by two inch substrate. However, the LEDs may be so tightly packed that each set of series-connected LEDs may include three hundred or more LEDs. The array preferably includes six sets of LEDs in a modular housing, although any number of sets or modules may be used in a particular application. In the preferred embodiment, two adjacent sets of LEDs are connected in series to yield an LED string of 68 LEDs. Three LED strings are connected in parallel to a DC power supply.

The LED array is preferably used in a modular housing that supports the array and that includes a cooling means such as a fan or an active heat sink for cooling the interior of the housing. A current regulator is capable of continuously varying the current to the array so that the emitted light from the array is equivalent to between about 0 to 2000 micromols per second per meter squared. The array is preferably covered with a glass cover to protect it from the environment.

The apparatus also preferably includes a means for briefly overriding the current regulator to provide maximum light output for a short period of time, on the order of 0.3 to 2 seconds. This override mode may be used to test for fluorescence of a plant leaf in a leaf chamber.

The array according to the present invention includes a number of features and advantages not found in prior art electrical energy sources. First, the array is inexpensive to manufacture using readily-available semiconductor chip manufacturing techniques, thereby avoiding the need to plug discrete LED components into a circuit board as in prior art devices. Second, the LEDs in the present array may be very tightly packed to achieve a light intensity output with minimal heat output when compared to metal halide and similar prior art devices.

A third advantage is that the LEDs may output the full spectrum of visible light, or may output any selected band or bands of monochromatic light as desired.

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Yet another advantage is that the light intensity may be continuously varied from a zero output up to a maximum output, which may equal or exceed the equivalent of one sun output (2000 micromols per second per meter squared) from an array that is only 3 inches by 4 inches in size.

The housings in which the arrays are disposed may be used separately or as modular components of a larger system. Each modular unit draws approximately 45 watts of power, compared to metal halide lamps which draw between about 150 to 1000 watts.

Other features and advantages of the present invention will be apparent to those skilled in the art from the following detailed description of the preferred embodiments and the attached drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of an LED array according to the present invention.

FIG. 2 is an exploded perspective view of a portion of the array of FIG. 1.

FIG. 3 is a perspective view of a single light emitting diode and adjacent conductive strips.

FIG. 4 is a perspective view of a modular housing according to the present invention.

FIG. 5 is a cross sectional side view of the modular housing, taken along line 5—5 of FIG. 4.

FIG. 6 is a schematic diagram depicting the power supply, the current regulator, and the override means of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 depicts an array of light emitting diodes (LEDs) according to the present invention though the description herein refers to LEDs, it is to be understood that other optoelectronic devices may be used, such as cold cathode fluorescent devices. In FIG. 1, array 10 includes an aluminum or copper-coated substrate 12 that acts as a heat sink for heat generated by LEDs 14. A layer 16 of a substantially non-electrically conductive material is formed on substrate 12. Layer 16 is preferably made of a ceramic material, although other materials may be used.

LEDs 14 are preferably grouped into a plurality of sets 18 and 20, with the LEDs in each set being series-connected. Each of sets 18 and 20 preferably occupies a one inch by two inch area of substrate 12, so that adjacent sets 18 and 20 occupy a two inch by two inch square area. This arrangement allows a commercially available extruded aluminum heat sink to be used for substrate 12. Sets 18 and 20 are preferably connected in series to yield an LED string of series-connected LEDs 14. Array 10 may consist of any number of sets of LEDs, with six sets of LEDs being preferred in a single modular housing, as depicted in FIG. 4.

As discussed below in connection with FIG. 6, each set 18 and 20 has two contacts. Set 18 has contacts 18a and 18b. Set 20 has contacts 20a and 20b. DC power is applied to contacts 18a and/or 20a, depending upon whether sets 18 and 20 are connected in series or in parallel to each other. The current through the LEDs is regulated by control signals applied to contacts 18b and/or 20b.

As depicted in FIG. 1, each of sets 18 and 20 includes 34 LEDs 14. However, the LEDs may be much more tightly packed, so that up to 300 or more LEDs may be series-connected into a single set.

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The manner in which the LEDs are connected to each other is more clearly depicted in FIGS. 2 and 3. In FIGS. 2 and 3, an exemplary LED 14a includes a substantially transparent double heterojunction 14b, an electrode 14c, and a cathode electrode 14d. The electrodes may be reversed so that electrode 14c is a cathode and electrode 14d is an anode, depending upon the choice of manufacturer for LED 14a. Heterojunction 14b is preferably made from a material containing gallium aluminum arsenide that is applied in epitaxial layers. Gallium aluminum arsenide is particularly suitable to yield a monochromatic light emission output in 620–680 and/or 700–760 nanometer ranges. Silicon carbide could be used to achieve a range of between 400–500 nm wavelength. The GaAlAs LEDs are preferably made by Mitsubishi Kaisi Polytech of Japan, and are available from Showa Denkoa or Stanley, both of Japan, or from Hewlett-Packard of Palo Alto, Calif. The silicon carbide LEDs are available from Cree Research Inc., Durham, N.C.

Heterojunction 14b is preferably encased in a passivation material 14e and is bonded to ceramic layer 16 using an electrically-conductive epoxy. One suitable epoxy adhesive is made by Ablestik of Rancho Dominguez, Calif., sold under the trademark ABLEBOND, Type No. 84-1LMIT. Ceramic layer 16 is preferably 10 mils thick, and is bonded to substrate 12 using a conductive epoxy made by Ablestik, sold under the trademark ABLEBOND, Type No. 789-4. Heat is transferred through ceramic layer 16 to the heat sink substrate 12.

Adjacent, series-connected LEDs 14 are connected to each other by means of electrically-conductive interconnects, such as strips 22 and standard wires 24. Strips 22 are preferably made from a metal ink. Other interconnects may be used in place of strips 22, such as a metal lead frame or metal wires.

In FIG. 2, strip 22a has a first end 22b that is electrically connected to cathode 14d, and an opposite second end 22c that is connected to one end 24b of wire 24a. The opposite end 24c of wire 24a is connected to the anode of an adjacent LED 14'. LED 14' and LED 14'', as well as the other series-connected LEDs 14 in array 10, are connected to each other in a manner similar to that discussed above in connection with LEDs 14a and 14'. FIG. 3 more clearly depicts the components of LED 14a.

The array of LEDs discussed above in connection with FIGS. 1 through 3 is preferably used to enhance or test plant growth. In these applications, LEDs 14 are preferably monochromatic, or output several narrow bands of spectral radiation, as disclosed in U.S. Pat. No. 5,012,609 to Ignatius et al., which patent is incorporated by reference herein. However, the LED array may have other applications, such as the irradiation of animal or human tissue. In the latter applications, the LEDs may be selected to provide different ranges of spectral emissions, as desired.

FIGS. 4 and 5 depict LED array 10 being housed in a modular unit 26 that is particularly suitable for enhancing plant growth. These modular units may be connected in parallel to provide a large scale artificial lighting environment for plants.

In FIGS. 4 and 5, modular unit 26 includes a housing 28 that supports LED array 10. A plurality of air vents 30 are formed in at least one side of housing 28. Modular unit 26 also includes a connector 32 that is adapted to receive a power cord from a power supply unit (not

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shown). Connector 32 is preferably a 16 pin connector, although only 10 pins are used in the embodiment discussed herein.

FIG. 5 is a side cross sectional view of modular unit 26, taken along line 5—5 of FIG. 4. In FIG. 5, modular unit 26 includes a glass cover plate 34 that protects LED array 10 from the environment. Disposed directly below LED array 10 is an internal heat sink 36 that has a plurality of fins or vanes 38 from which heat generated by LED array 10 is dissipated. An internal fan 40 pulls the heat from the interior of housing 28 and propels it into the environment.

Also disposed within housing 28 is a circuit board 42 that contains at least some of the components of the internal DC power supply, the current regulator, and override circuit discussed below in connection with FIG. 6. The remaining electronics may be contained in a separate control unit.

In FIG. 6, 120 VAC is input to the circuits at connector 33. A fuse 44 and a current limiter 46 protect the electronics from power surges, voltage spikes and the like. The input AC waveform is rectified by a half-wave rectifier consisting of diode 48, capacitor 50, and resistor 52. The output from the rectifier is +180 V direct current. The unrectified AC signal is used to power fan 40 via lines 54 and 56. The AC signal is also used to drive a converter 58, whose output on line 60 is +5 VDC that is used to drive the circuit logic.

The +180 VDC is input to LED array 10 via lines 62, 64, 66, and 68. In the preferred embodiment described herein, the LED array, consisting of 6 sets of series-connected LEDs 14, is divided into 3 LED strings 70, 72, and 74, with the LEDs in each string being series-connected. Two adjacent LED sets are connected in series to form each LED string. LED strings 70, 72, and 74 are connected to each other in parallel.

The current through LED strings 70, 72, and 74 is precisely controlled by a constant current regulator consisting of circuits 76, 78, and 80 respectively. Regulator circuit 76 includes an operational amplifier 76a whose positive input is a voltage reference signal Vref that is derived as discussed below. The output of amplifier 76a controls the gating of a Darlington transistor pair 76b which in turn controls the current through LED string 70. The emitter of Darlington pair 76b is connected to the negative input of amplifier 76a to provide current feedback, as is well known in the art.

Current regulator circuits 78 and 80 have similar configurations to current regulator circuit 76. Regulator circuit 78 includes an operational amplifier 78a whose positive input is the signal Vref, and whose negative input is the feedback signal from Darlington transistor pair 78b. Operational amplifier 78a controls the gating of transistor pair 78b, which in turn precisely controls the current through LED string 72.

Similarly, regulator circuit 80 includes an operational amplifier 80a whose positive input receives the signal Vref, and whose negative input receives a current feedback signal from the emitter of a Darlington pair 80b. Darlington transistor 80b controls the current through LED string 74.

The voltage reference signal Vref that is used to regulate the current in the LEDs is derived from the manual setting of a continuously variable pot switch 82 located on the front panel of the control unit. Switch 82 is continuously variable from 0 to 100 milliamps. Switch 82 is connected in series with the source of a normally ON field effect transistor (FET) 84. When switch 84 is

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ON, the setting of switch 82 forms a voltage divider between the full scale calibration pot switch 102 and resistor 108 to determine the Vref signal, the latter varying from 0 volts (corresponding to 0 milliamps) to 1 volt (corresponding to a 100 milliamp setting of switch 82).

The present invention also includes a means for briefly overriding the setting of switch 82 to achieve a maximum or "overdrive" output from the LED array for a brief period of time, on the order of 0.3 to 2 seconds. In the embodiment discussed herein, the setting of switch 82 is overridden for a period of 1 second. This feature may be used to test the fluorescence of a plant leaf by placing the leaf in a leaf chamber (not shown) in close proximity to array 10 of modular unit 26.

In FIG. 6, the override circuit includes a front panel switch 86, NOR gate 88, inverters 90, 92 and 94, a 556 timer (depicted as dual 555 timers 96 and 98), an FET 100, resistors 109 and 111, and a pot switch 102 which is calibrated to full scale.

The override circuit operates as follows. When switch 86 is pressed, input 88a of NOR gate 88 is brought to a low state. Since input 88b is also in a low state when switch 86 is depressed for the first time, the output of gate 88 becomes a high input to gate 90, which is connected as an inverter. The output of inverter 90 goes low, triggering delay circuit 96 and overdrive circuit 98.

After the override circuit has been successfully triggered, delay circuit 96 outputs a high state signal at pin 5 for 30 seconds to prevent the retriggering of the circuit, regardless of whether switch 86 is pressed during that delay period. Delay circuit 96 outputs a high state signal to input 88b of NOR gate 88, causing the output of NOR gate 88 and the input to inverter 90 to go low. The output of inverter 90 goes high, thereby preventing the triggering of overdrive circuit 98 during the delay period.

The high state signal from pin 5 of delay circuit 96 is inverted by inverter 92, causing LED 104 to remain OFF. LED 104 is a front panel light which indicates whether the override mechanism is in the Ready state.

After pin 8 of overdrive circuit 98 receives a low going trigger signal, overdrive circuit 98 outputs at pin 9 a high state signal to gate ON FET 100. The gating ON of FET 100 switches resistors 109 and 111 to line 106 to form a voltage divider between full scale calibration pot 102 and resistor 108, resulting in a maximum value for the voltage reference signal Vref. Regulator circuits 76, 78, and 80 then allow maximum current to flow through their respective LED strings 70, 72 and 74.

The high state signal output at pin 9 of overdrive circuit 98 is inverted by inverter 94, the latter outputting a low state signal to turn OFF FET 84. The turning OFF of FET 84 deactivates pot switch 82 for a 1 second time period during the operation of the override circuit.

After the 30 second delay period has ended, input 88b to NOR gate 88 goes low. Input 88a to NOR gate 88 is high as a result of pull-up resistor 110. The output of NOR gate 88 is thus low, and the output of inverter 90 goes high, thereby preventing the triggering of delay circuit 96 and overdrive circuit 98 until switch 86 is activated again.

Although several preferred embodiments of the present invention have been shown and described, other embodiments will be apparent to those skilled in the art and are within the intended scope of the present inven-

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tion. Therefore, the invention is to be limited only by the following claims.

We claim:

1. An array of optoelectronic devices comprising:
 - a thermally-conductive substrate;
 - a substantially non-electrically conductive layer disposed on said substrate;
 - a first optoelectronic device disposed on said layer, including
 - at least one first heterojunction;
 - a first electrode interconnected with said first heterojunction;
 - a second electrode interconnected with said first heterojunction;
 - a second optoelectronic device disposed on said layer and connected in series with said first optoelectronic device, said second optoelectronic device including
 - at least one second heterojunction;
 - a third electrode interconnected with said second heterojunction;
 - a fourth electrode interconnected with said second heterojunction;
 - a first electrically-conductive interconnect disposed above said substantially non-conductive layer having a first end in electrical connection with said first electrode and having an opposite interconnect end in electrical connection with said fourth electrode;
 - a regulator that is adapted to continuously vary the output of said first and second optoelectronic devices; and

override means for briefly overriding said regulator to thereby briefly increase the output of said first and second optoelectronic devices.
2. The array of claim 1, wherein said thermally-conductive substrate is made from a material containing a metal.
3. The array of claim 2, wherein said metal is aluminum or copper.
4. The array of claim 1, wherein said substantially non-electrically conductive material includes a ceramic material.
5. The array of claim 1, wherein said electrically-conductive interconnect is made from a conductive ink.
6. The array of claim 1, further comprising:
 - a wire connected between said opposite interconnect end and said fourth electrode.
7. The array of claim 1, wherein said at least one first heterojunction includes two heterojunctions.
8. The array of claim 1, wherein said first heterojunction includes a plurality of epitaxial layers.
9. The array of claim 1, wherein said first and second optoelectronic devices are substantially monochromatic.
10. The array of claim 9, wherein said monochromatic devices have a peak wavelength emission in the range of 620 to 680 nanometers.
11. The array of claim 1, wherein said first heterojunction is substantially enclosed in a passivation material.
12. The array of claim 1, wherein said first heterojunction is made from a material containing at least one of gallium aluminum arsenide and silicon carbide.
13. The array of claim 1, further comprising:
 - a protective coating disposed on said first and second optoelectronic devices and on said interconnect.

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14. The array of claim 1, wherein said first and second optoelectronic devices are light emitting diodes.

15. The array of claim 1, wherein said first electrode and said third electrode have a first polarity, and wherein said second electrode and said fourth electrode have a second polarity opposite to said first polarity.

16. The array of claim 1, further comprising:

- a third optoelectronic device connected in series with said second optoelectronic device, including a fifth electrode and a sixth electrode;
- a second electrically-conductive interconnect disposed above said layer having a first end in electrical connection with said third electrode and having an opposite second interconnect end in electrical connection with said sixth electrode.

17. The apparatus of claim 1, wherein said override means includes:

means for providing maximum output of said first and second optoelectronic devices for a period of 0.3 to 2 seconds.

18. An apparatus that provides radiant energy to at least one living cell, comprising:

- a housing;
- an array of optoelectronic devices disposed within and supported by said housing, said array including
 - a thermally-conductive substrate;
 - a substantially non-electrically conductive layer disposed on said substrate;
 - a first optoelectronic device disposed on said layer and having a first electrode and a second electrode;
 - a second optoelectronic device disposed on said layer and having a third electrode and a fourth electrode;
 - a conductive interconnect disposed above said layer having one end electrically connected to said first electrode and having an opposite end electrically connected to said fourth electrode;
- a power source that supplies power to said array;
- a regulator that is adapted to continually vary the energy emitted from said array; and
- override means for briefly overriding said regulator to thereby briefly increase the energy emitted by said array.

19. The apparatus of claim 18, wherein said first and second optoelectronic devices are light emitting diodes.

20. The apparatus of claim 18, wherein said first electrode and said third electrode have a first polarity, and wherein said second electrode and said fourth electrode have a second polarity opposite to said first polarity.

21. The apparatus of claim 18 wherein said housing has an interior, said apparatus, further comprising:

cooling means for removing heat from the interior of said housing that was transferred from said optoelectronic devices through said thermally-conductive substrate.

22. The apparatus of claim 21, wherein said cooling means includes a fan interconnected with said housing.

23. The apparatus of claim 18, wherein said power source is a DC power supply.

24. The apparatus of claim 18, wherein said radiant energy includes emitted light, and wherein said regulator is adapted to continuously vary said emitted light from between 0 to 2000 micromols per second per meter squared.

25. The apparatus of claim 18, wherein said override means includes:

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means for providing maximum energy output for a period of 0.3 to 2 seconds.

26. The apparatus of claim 18, further comprising:

a glass cover disposed above said array and supported by said housing.

27. The apparatus of claim 18, wherein said array includes a plurality of sets of optoelectronic devices, each of said sets having at least two series-connected optoelectronic devices connected by a conductive interconnect.

28. The apparatus of claim 18, wherein said thermally-conductive substrate is made from a material containing a metal.

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29. The apparatus of claim 18, wherein said substantially non-electrically conductive material includes a ceramic material.

30. The apparatus of claim 18, wherein said electrically-conductive interconnect is made from a conductive ink.

31. The apparatus of claim 18, wherein said first and second optoelectronic devices are substantially monochromatic.

32. The apparatus of claim 31, wherein said monochromatic devices have a peak wavelength emission in the range of 620 to 680 nanometers.

33. The apparatus of claim 18, further comprising: a protective coating disposed on said first and second optoelectronic devices and on said conductive interconnect.

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EXHIBIT U-5

(12) **United States Patent**
Popovich et al.

(10) **Patent No.:** **US 6,582,103 B1**
(45) **Date of Patent:** **Jun. 24, 2003**

(54) **LIGHTING APPARATUS**

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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

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(22) Filed: **Jul. 20, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 08/936,717, filed on
Sep. 24, 1997, which is a continuation-in-part of application
No. 08/764,298, filed on Dec. 12, 1996, now abandoned.
(60) Provisional application No. 60/144,920, filed on Jul. 21,
1999.

(51) **Int. Cl.**⁷ **F21V 7/00**

(52) **U.S. Cl.** **362/307; 361/31; 361/224;**
361/240; 361/245

(58) **Field of Search** 362/31, 27, 29,
362/555, 224, 249, 240, 238, 307, 244,
245

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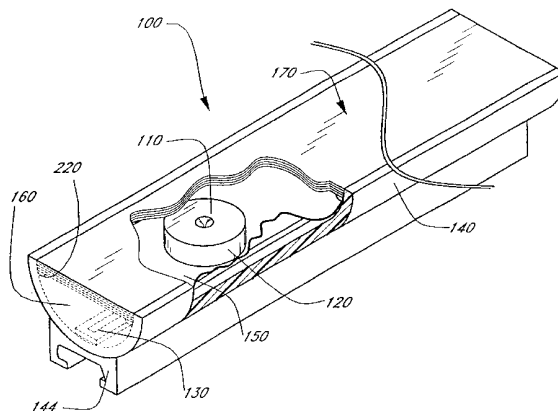
Assistant Examiner—Guiyoung Lee

(74) *Attorney, Agent, or Firm*—Kirkpatrick & Lockhart
LLP

(57) **ABSTRACT**

An illumination apparatus provides an output with high spatial uniformity of luminance. The illumination apparatus includes a cavity that has reflective surfaces and an output area. At least one light source is disposed in the cavity, with the light source including a point source (such as an LED) and an optical diverter having a flared (e.g., cusped) reflecting surface. Light from the point source is distributed by the optical diverter towards the reflective surfaces within the cavity. Before exiting the device, light passes through an optical conditioning element that is positioned over the output area of the cavity. The optical conditioning element includes at least a diffuser, such as a translucent film or plastic sheet, and preferably also includes one or more prism sheets such as a brightness-enhancing film.

52 Claims, 15 Drawing Sheets



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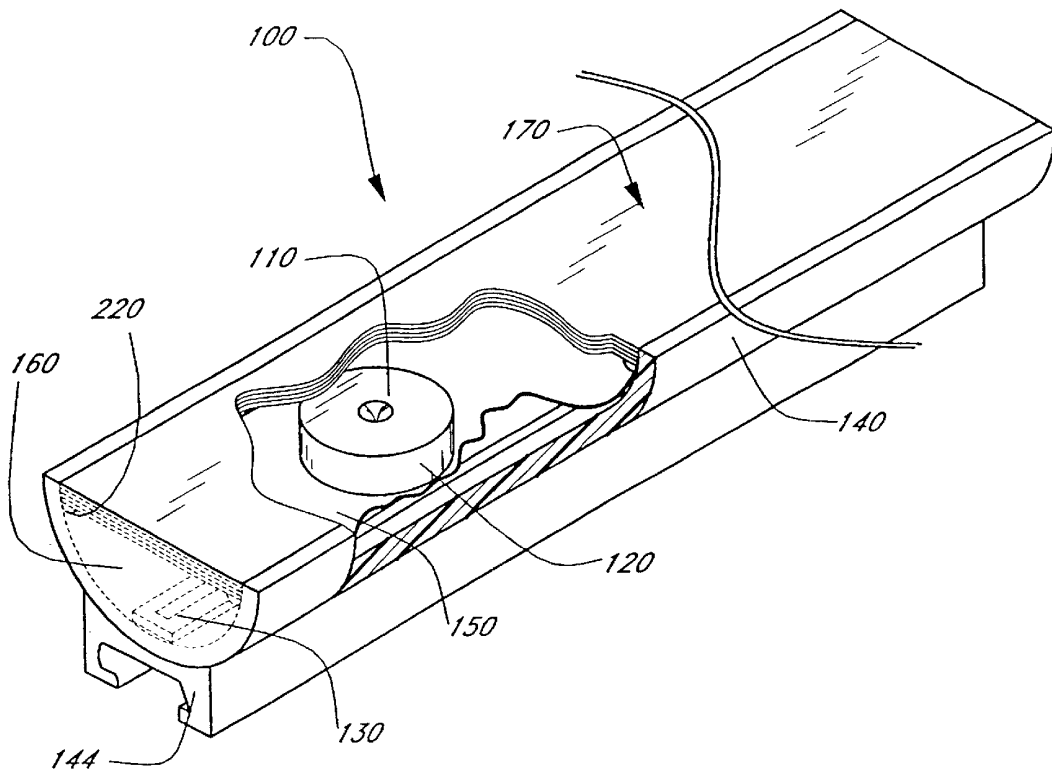
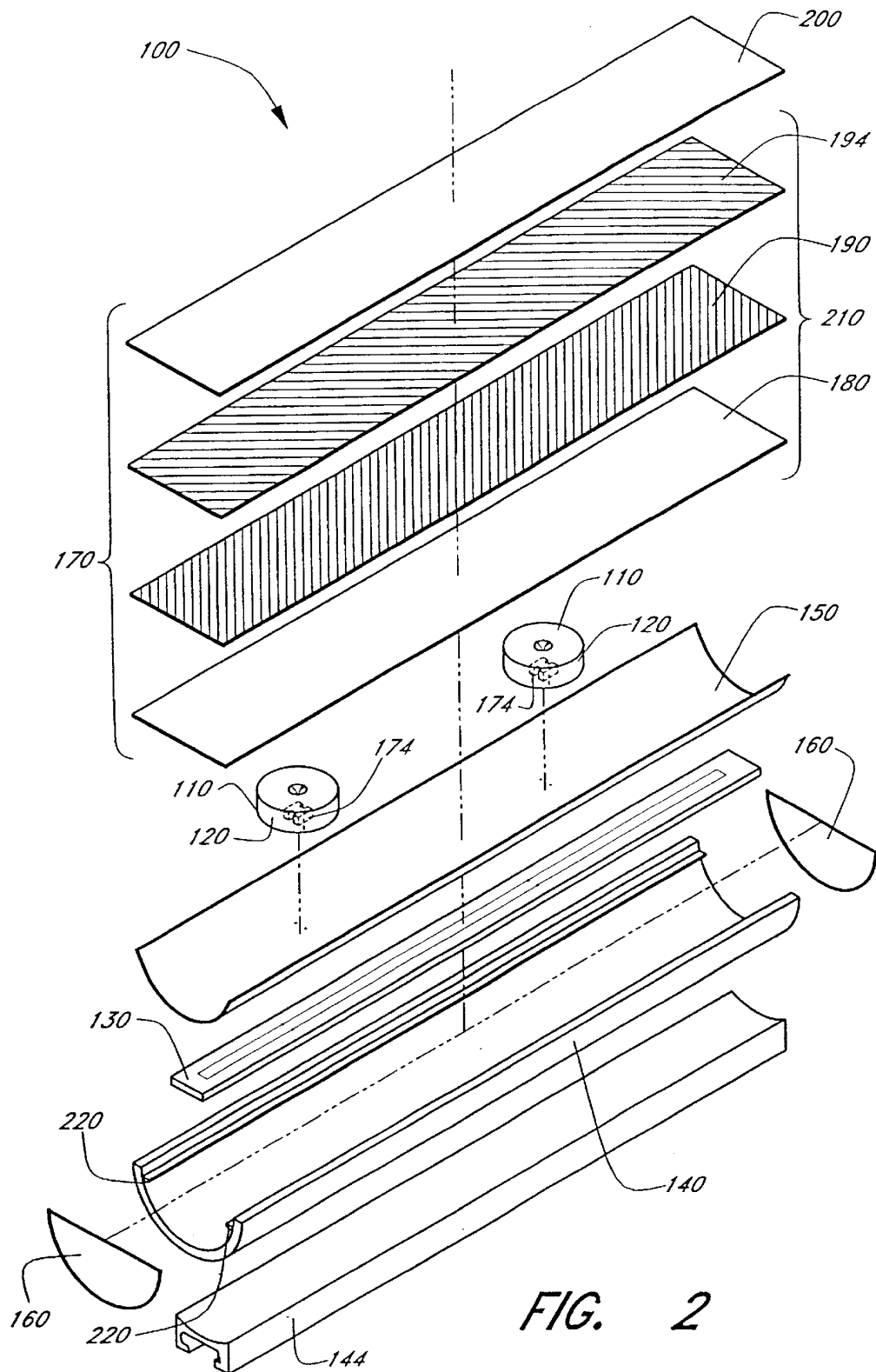


FIG. 1



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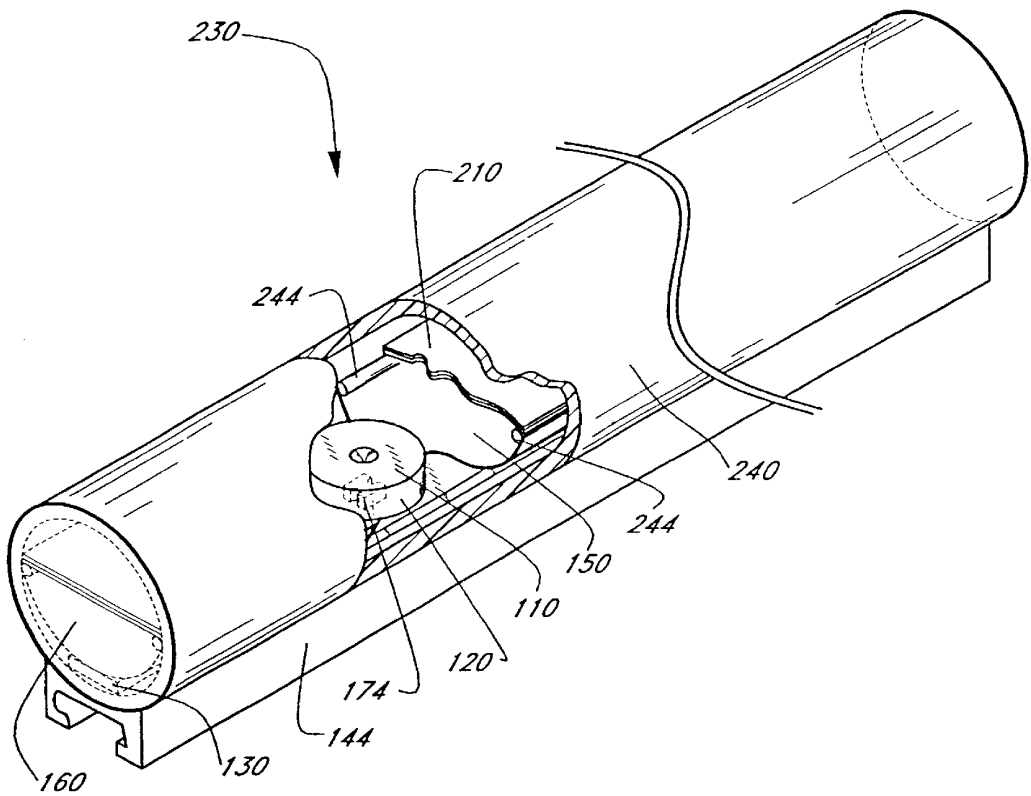


FIG. 3

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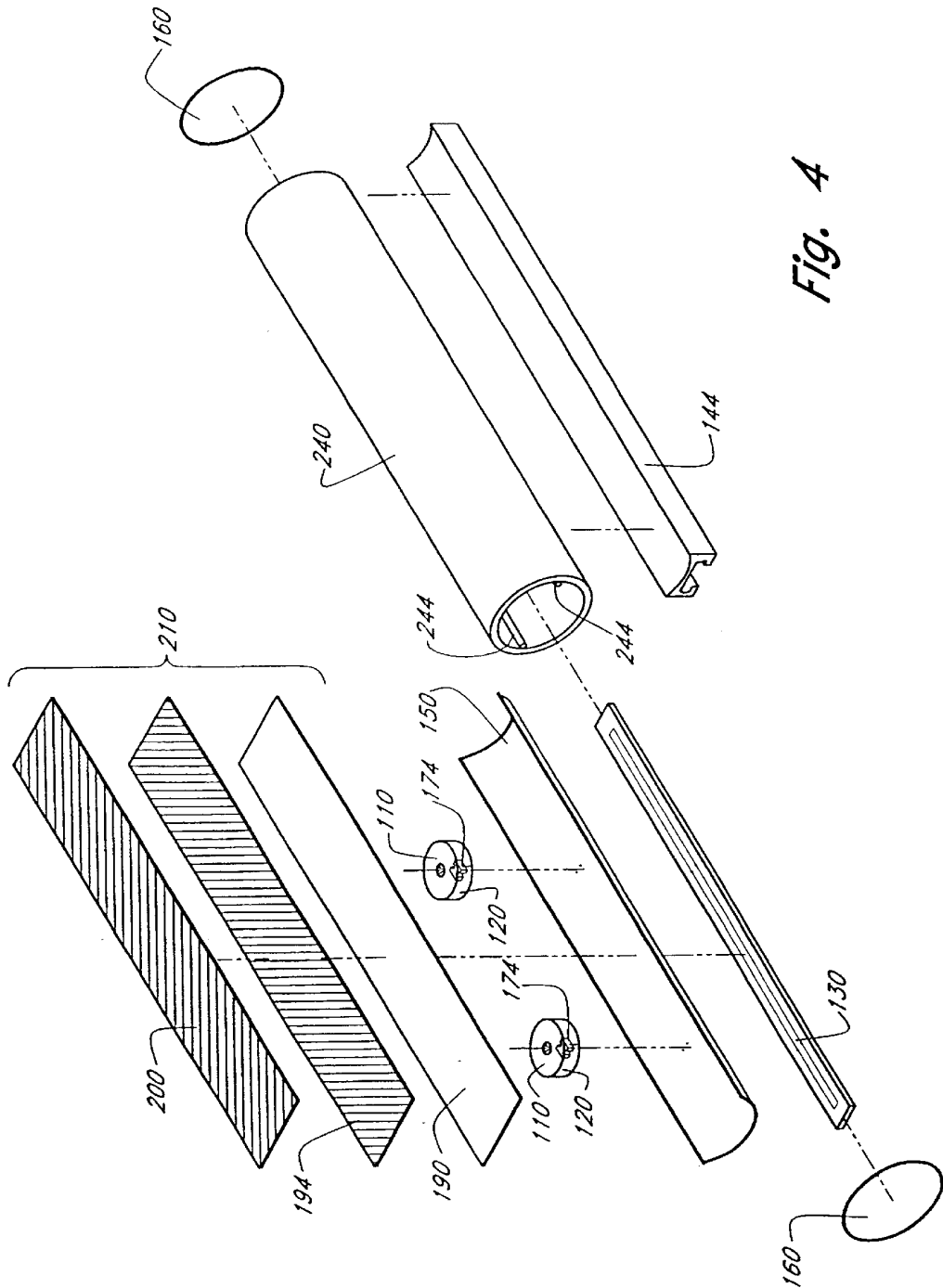


Fig. 4

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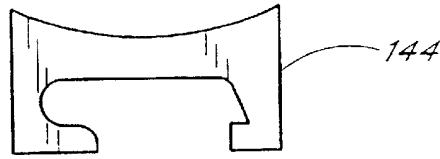


FIG. 5A

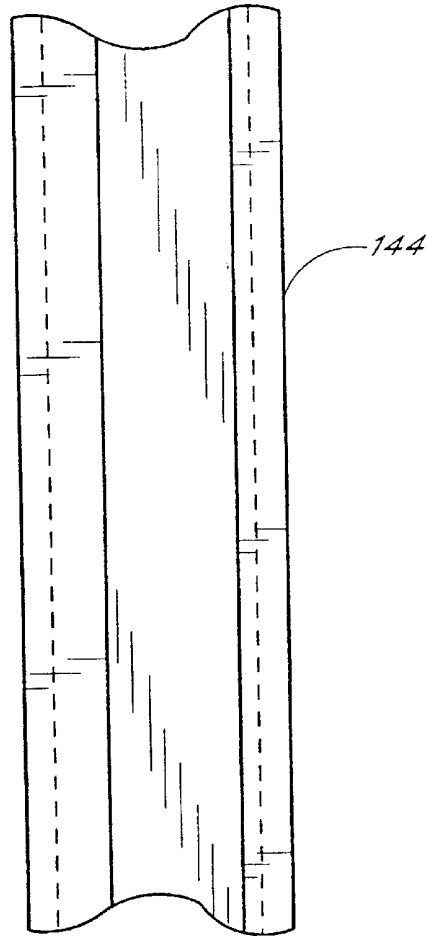


FIG. 5B

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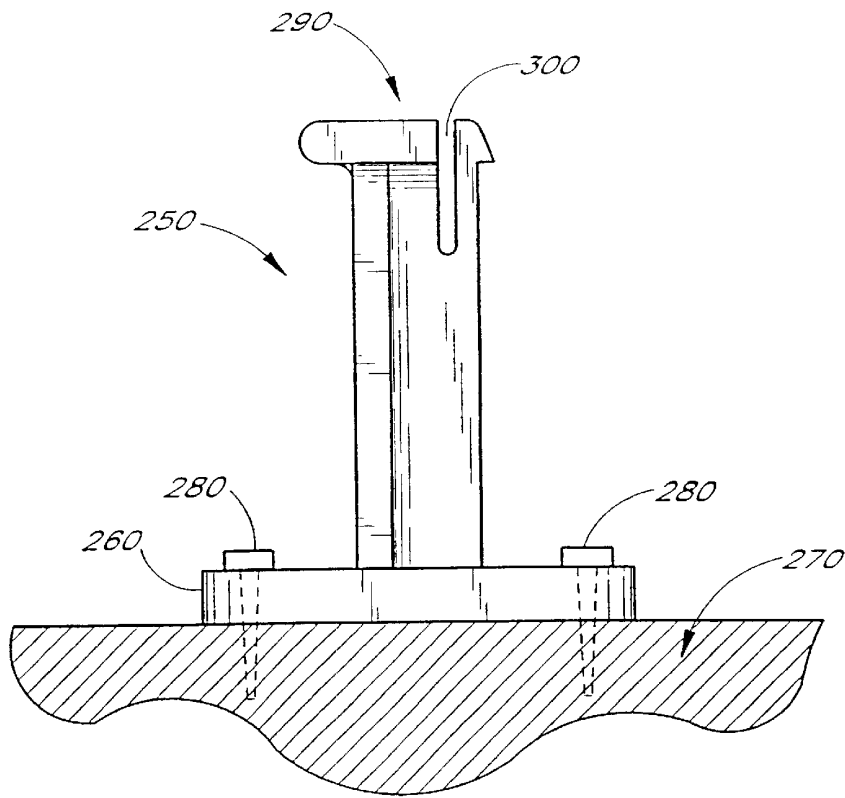


FIG. 6A

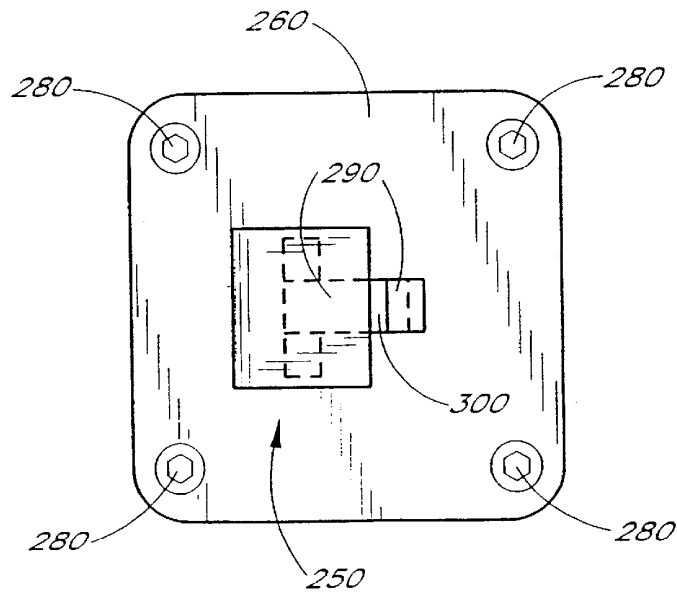


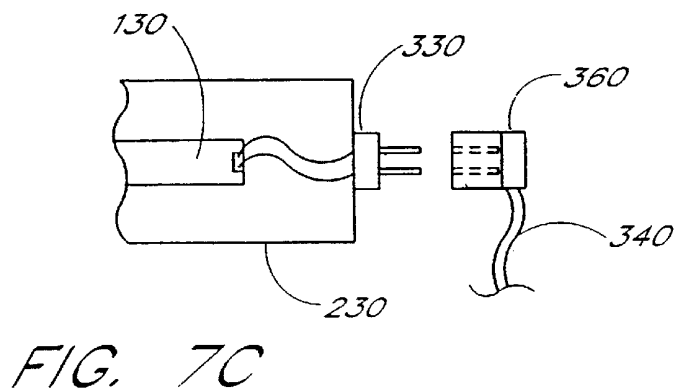
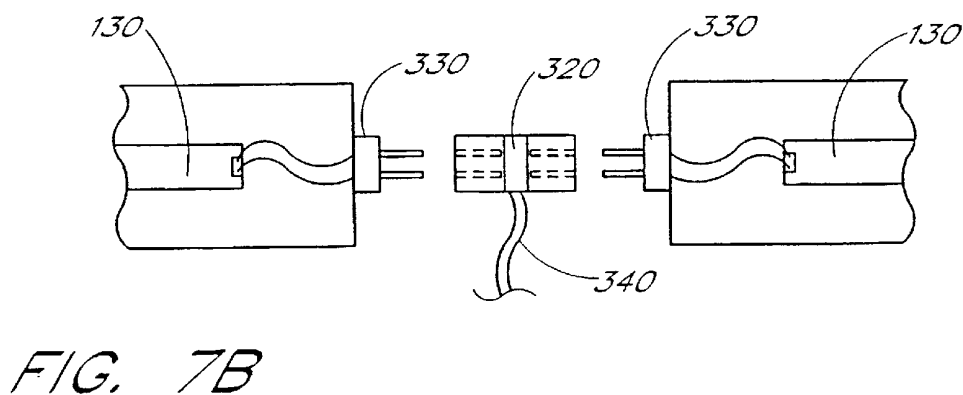
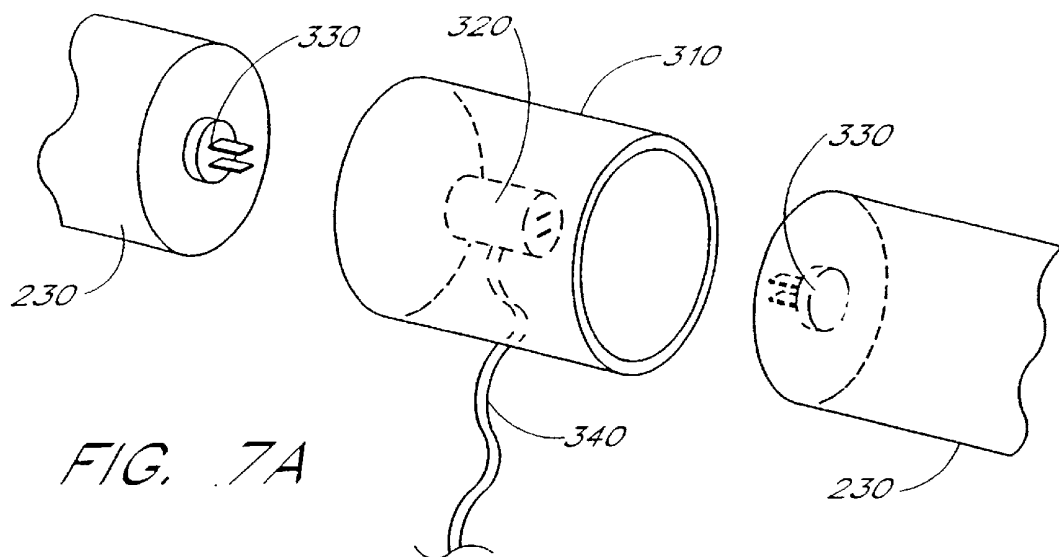
FIG. 6B

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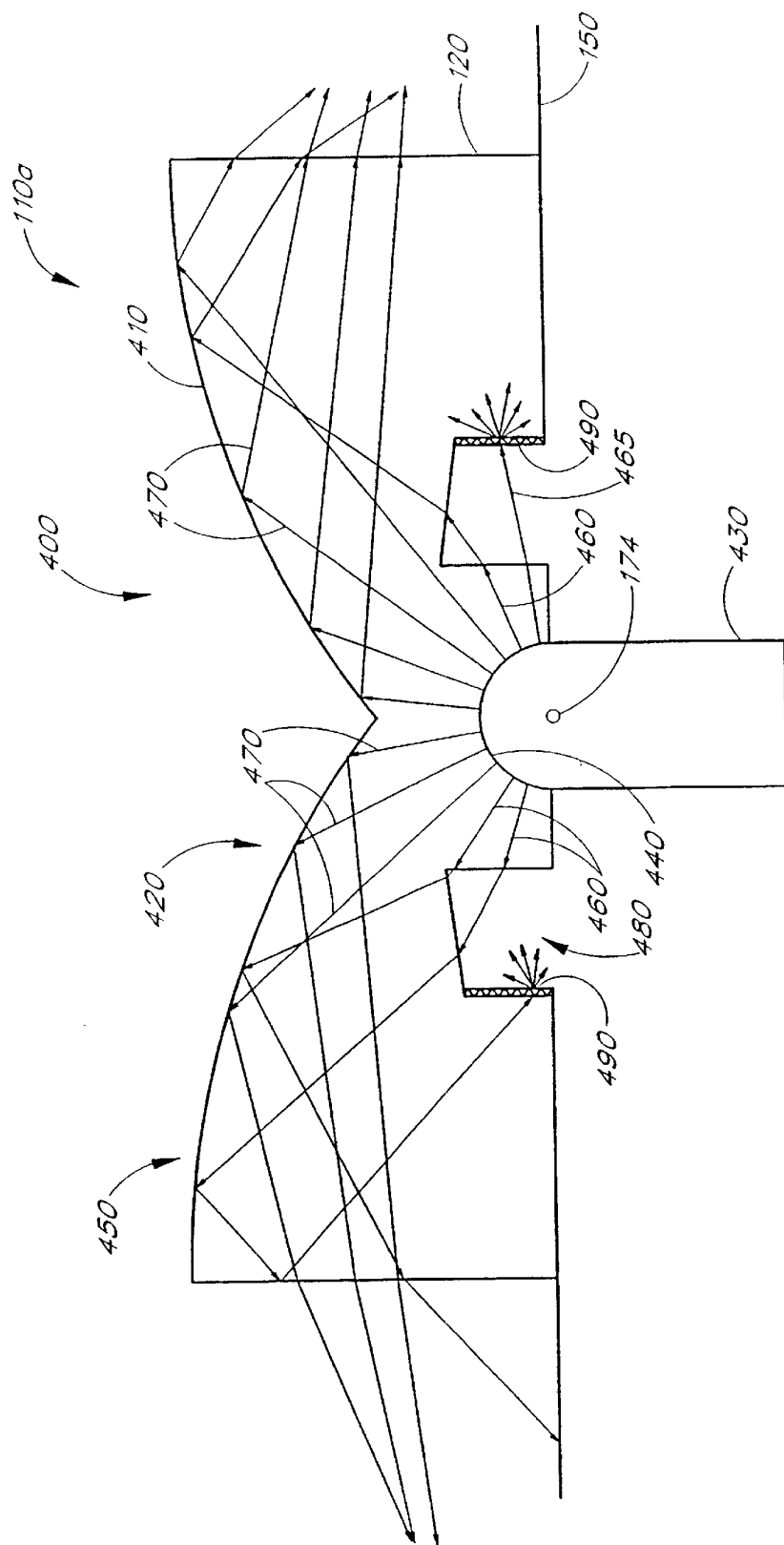


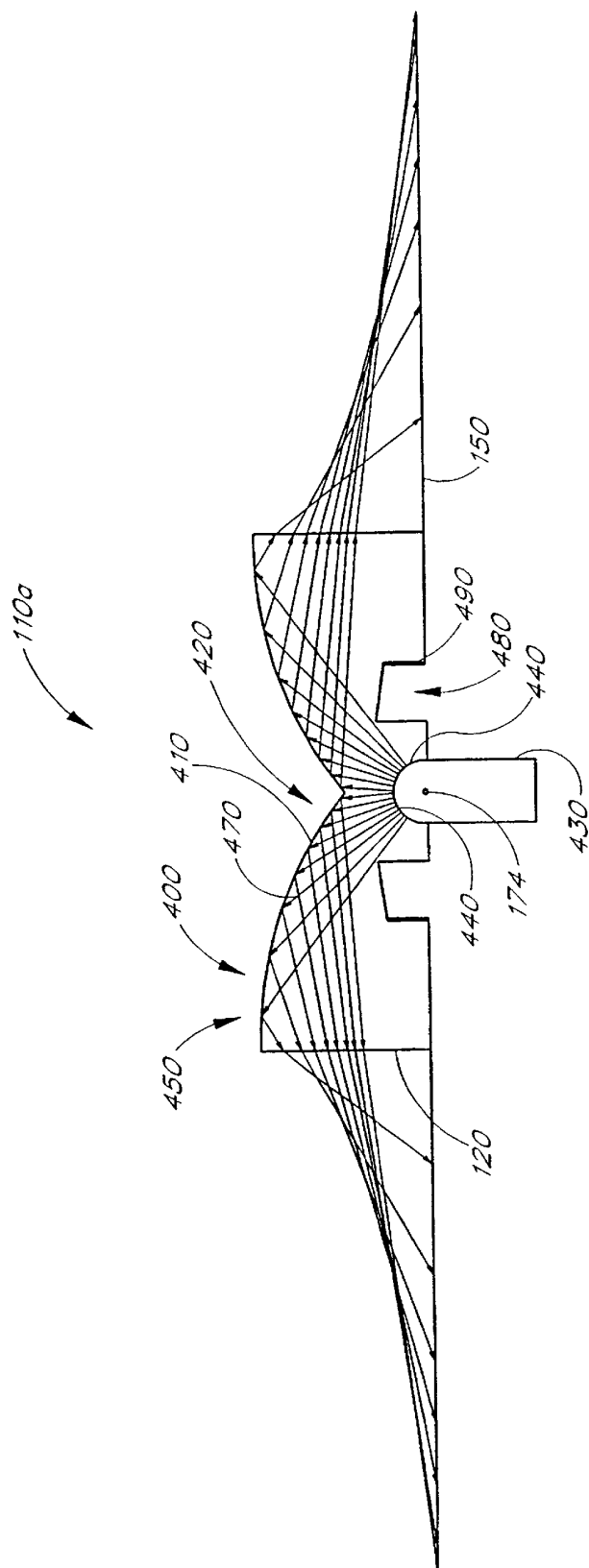
FIG. 9

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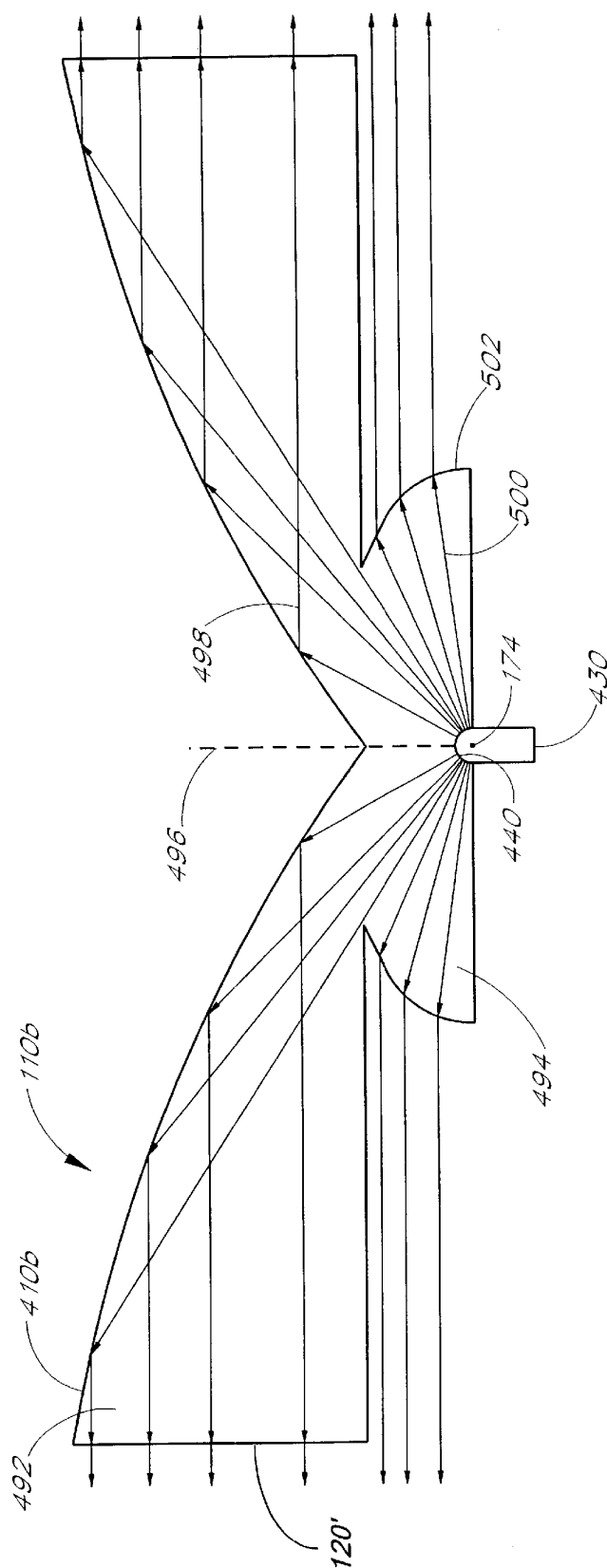


FIG. 12

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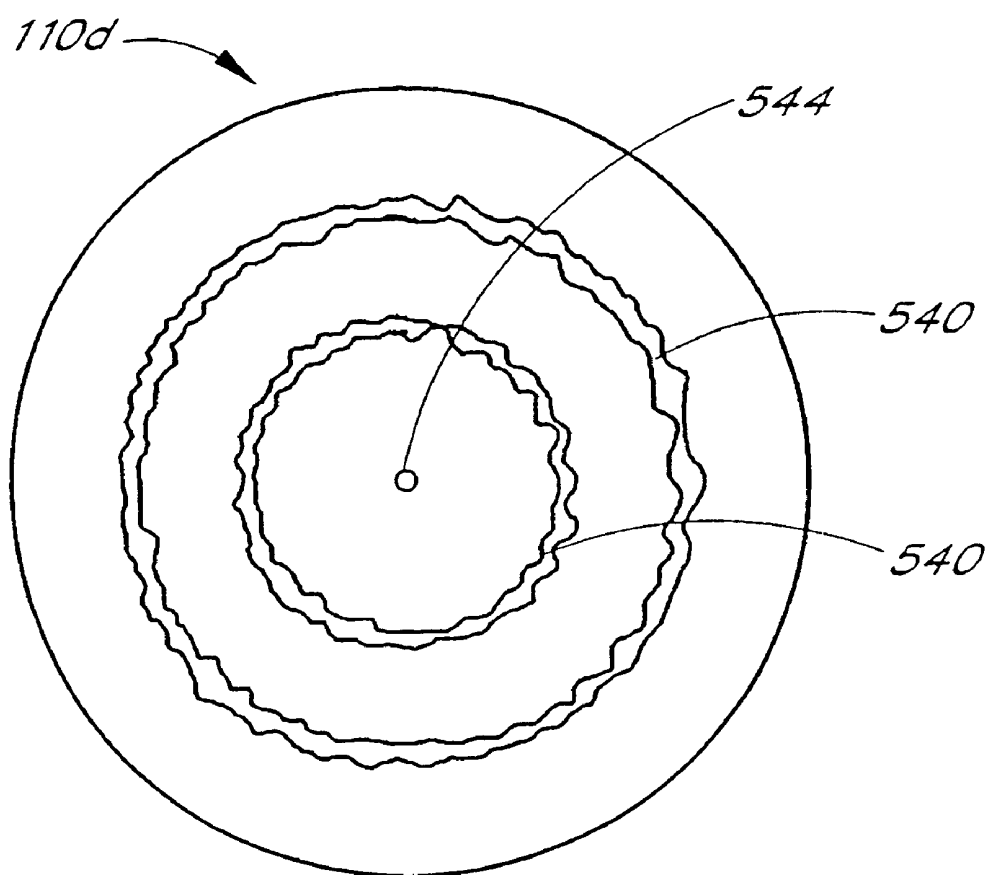


FIG. 14

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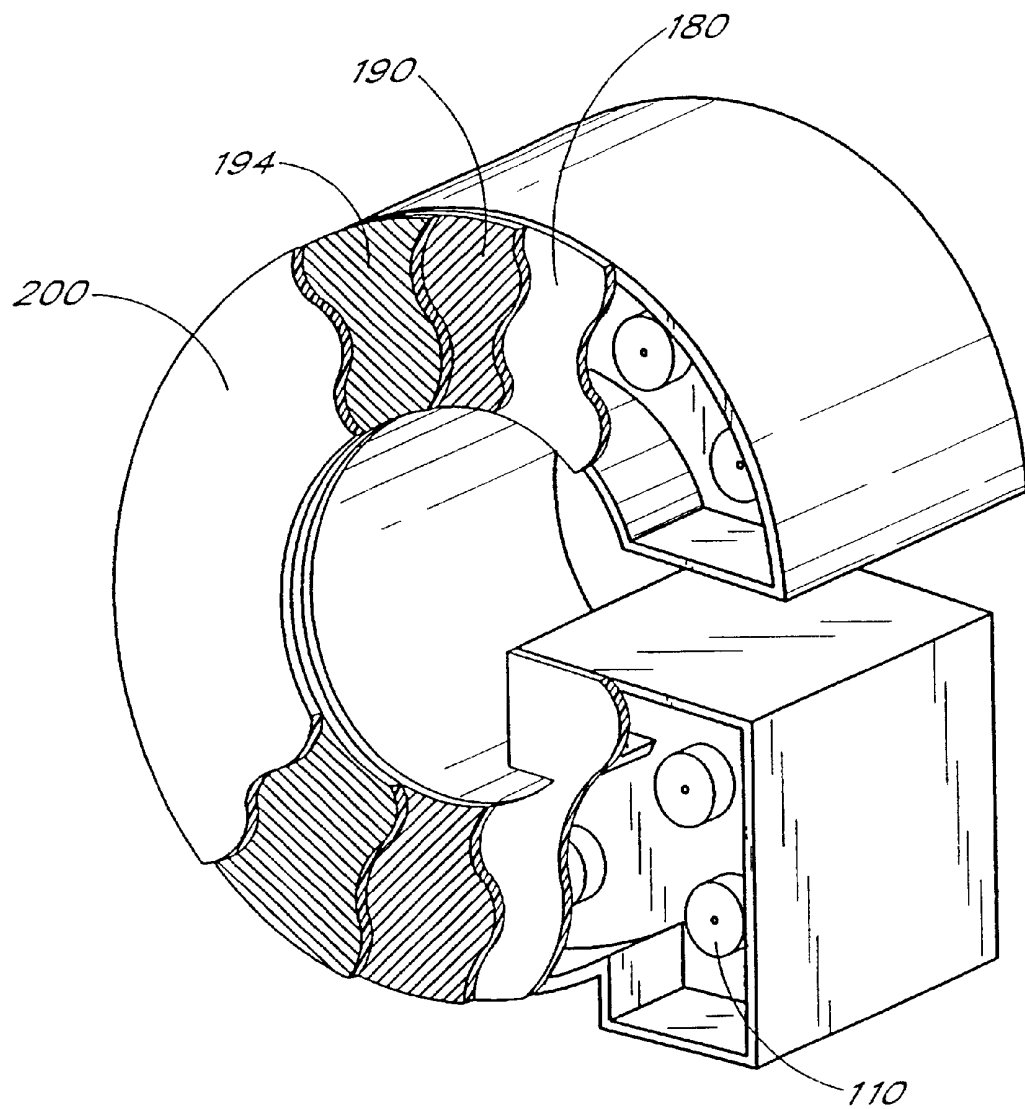


FIG. 15

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LIGHTING APPARATUS**BACKGROUND OF THE INVENTION**

This application claims the benefit of U.S. Provisional Application No. 60/144,920, filed Jul. 21, 1999 and is a continuation in part of application Ser. No. 08/936,717 filed Sep. 24, 1997, which in turn is a continuation in part of Application No. 08/764,298 filed Dec. 12, 1996, now abandoned all of which are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to the field of lighting devices, and more specifically to devices capable of a low profile which utilize point sources, such as light emitting diodes, for illumination.

DESCRIPTION OF THE RELATED ART

Low profile lighting devices are useful in a variety of applications, such as decorative strip lighting or display panel illumination. One common form of strip lighting utilizes neon tubes. Neon tubes have the advantages of being lightweight and lending themselves to decorative lighting. Further, the light output from neon tubes is relatively diffuse and uniform in appearance. However, neon tubes are fragile, require high voltage, and generate significant radio-frequency (RF) interference, which must often be shielded at significant cost. Fluorescent lighting is likewise diffuse, but is generally limited to short lengths and typically includes unattractive electrical connections.

Display panel illumination is often accomplished by placing light sources behind the panel to illuminate it. A diffuser box containing a light source can generate output that is fairly uniform, so long as the light sources are sufficiently far away from the display panel. This makes such devices bulky, however. If the light sources are too close to the panel, the illumination will no longer be uniform, and the sources will be seen as "hot spots." Thus there is a need for a compact lighting device that provides uniform output intensity.

SUMMARY OF THE INVENTION

According to one aspect of the invention, an illumination apparatus includes a cavity having reflective surfaces and an output area, as well as at least one light source disposed in the cavity, wherein the light source includes a point source and an optical diverter having a flared reflecting surface. The apparatus further includes an optical conditioning element over the output area, with the optical conditioning element including at least a diffuser, for example, a translucent film or plastic sheet. In a preferred embodiment, the flared surface is curved, and may be cusped. In one preferred embodiment, the point source comprises an LED. In a preferred embodiment, the cavity reflecting surfaces are diffusively reflective.

According to another aspect of the invention, an illumination apparatus comprises a housing that includes a cavity having reflective surfaces and an output aperture. The apparatus also includes an optical conditioning element across the output aperture, in which the conditioning element comprises at least one sheet having a plurality of pixels. The apparatus further includes at least one light source disposed within the cavity directly beneath the conditioning element, in which the (at least one) light source includes a point source spaced less than 3-½ inches from the sheet that illuminates the reflective surfaces such that the ratio of the luminance of adjacent pixels is between 0.95 and 1.05 and

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such that the ratio of the luminance of non-adjacent pixels is between 0.5 and 2.0, whereby the appearance of illumination at the sheet is substantially uniform. In a preferred embodiment, the optical conditioning element includes a diffuser sheet disposed below the prism sheet. In one preferred embodiment, the optical conditioning element includes a second prism sheet with orientation 90° from the first. In a preferred embodiment, the (at least one) light source includes a point source and a total internal reflection lens having a cusped surface for reflecting light from the point source against the diffusive reflective surfaces.

According to another aspect of the invention, an illumination apparatus includes a cavity formed by reflective material, in which the cavity has an output area. An optical conditioning element is at the output area. The apparatus further includes a light source in the cavity, in which the light source includes a point source and an optical diverter having a reflecting surface which is partially reflective and partially transmissive. The reflective surface of the diverter allows a portion of light incident thereon to pass through the reflecting surface, while reflecting another portion of the incident light onto the reflective material of the cavity. The reflective material reflects light within the cavity, whereby the output area and the optical conditioning element are illuminated. In a preferred embodiment, the reflecting surface of the diverter is comprised of scattering centers which scatter light incident thereon.

According to yet another aspect of the invention, an illumination apparatus includes an optical diverter. The diverter includes transparent material having a reflecting surface formed by a refractive index interface configured to totally internally reflect light from a point source positioned to emit a first portion of light rays towards the reflecting surface and a second portion of light rays towards a side surface of the diverter. The diverter includes a refracting interface that refracts the second portion of light rays towards the reflecting surface, such that both the first and second portions of light rays are reflected from the reflecting surface.

According to yet another aspect of the invention, there is provided an optical diverter that includes transparent material having a flared reflecting surface formed by a refractive index interface. The interface is configured to totally internally reflect light from a point source which is positioned adjacent to an apex of the flared reflecting surface and which emits light rays for reflection by the reflecting surface.

According to a further aspect of the invention, an illumination apparatus includes a cavity having reflective surfaces and an output area. The apparatus further includes at least one light source disposed in the cavity, in which the light source includes a point source and an optical diverter having a surface that is partially reflective and partially transmissive. The apparatus also includes an optical conditioning element over the output area, in which the optical conditioning element includes a diffuser, wherein the diverter is positioned between the point source and optical conditioning element such that (a) a portion of light emitted by the point source is reflected from the diverter towards the reflective surfaces of the cavity, and (b) another portion of light emitted by the point source is transmitted through the surface of the diverter towards the optical conditioning element, with the diverter sized to allow at least a substantial portion of the reflected light to reach the optical conditioning element without passing through the diverter, and wherein the diverter and the reflective surfaces of the cavity are arranged to allow at least a substantial portion of the transmitted light to reach the optical conditioning element without undergoing reflection.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a first embodiment of a low profile lighting device with the housing partially cut away to reveal one of the point light sources and optical diverters therein.

FIG. 2 is an exploded view of the embodiment illustrated in FIG. 1.

FIG. 3 shows another embodiment of a low profile lighting device.

FIG. 4 is an exploded view of the embodiment illustrated in FIG. 3.

FIGS. 5A and 5B are end and plan views, respectively, of a mounting channel having a slot for mounting the embodiment of FIGS. 1-2 or FIGS. 3-4 to the mounting bracket of FIGS. 6A and 6B.

FIGS. 6A and 6B are elevation and plan views, respectively, of a mounting bracket which is secured to a mechanical structure such as a building, and which receives the mounting channel of FIGS. 5A and 5B to mount the low profile lighting device on the building.

FIGS. 7A and 7B show a collar for mechanically and electrically coupling two lighting devices.

FIG. 7C shows an electrical arrangement for coupling power to an end of a lighting device.

FIG. 8 shows an optical diverter which utilizes total internal reflection for laterally diverting light from a light emitting diode or other point source.

FIGS. 9, 10, and 11 show the progression of light rays through the optical diverter of FIG. 8.

FIG. 12 shows an optical diverter which produces highly collimated "equatorial" output beam.

FIG. 13 shows the progression of light rays through an optical diverter having scattering centers on its top surface for diffusely transmitting some light through the top surface.

FIG. 14 shows an optical diverter having a roughened surface pattern in the form of a series concentric rings on its top surface for diffusely transmitting some light through the top surface.

FIG. 15 shows an embodiment of a lighting device in the form of an alphanumeric character.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

One preferred embodiment of a lighting device 100, illustrated in FIG. 1, comprises a plural light sources, each of which includes a point source such as a light emitting diode (LED) shown in FIG. 8, and an optical diverter 110. Light from the LED 174 is received by the optical diverter 110 which redirects the light laterally and downwardly. The plural LEDs are coupled to each other electrically by a printed circuit board 130 (a wire harness is an alternative configuration). The point sources 174 and optical diverters 110 are mounted within an elongate cavity formed by a sheet 150 of diffusively reflective material in the general form of a half or hemi cylinder. The sheet 150 is mounted in, and extends the length of, a housing 140, which may be an extrusion. The housing 140 is generally elongate and has a width that is not substantially greater than the width of the light output area. The printed circuit board 130 is disposed between the sheet 150 and the bottom of the housing 140. Wires (not shown) pass through the sheet 150 to electrically connect the point sources to the circuit board. A mounting channel 144 may be included on the bottom of the housing 140 for mounting the device 100 to a building. The mounting channel 144 may, for example, be made of acrylic that is

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bounded or glued to the housing 140, or the channel 144 may be integrally formed with the housing 140 as part of an extrusion process. The light that exits the diverters 110 is reflected by the diffusely reflecting sheet 150, located between the optical diverters 110 and the circuit board 130, as well as by diffusely reflecting end caps 160 connected to the housing 140 at either end of the device 100. If a plurality of optical diverters 110 are linearly arranged along the longitudinal axis of the cavity, the maximum separation between adjacent optical diverters 110 is preferably about twice the width of the device 100. Further, the optical diverters 110 are preferably separated by at least 0.5 inches. Surfaces of the diffusely reflecting sheet 150 and the diffusely reflecting end caps 160 are preferably matte white, with diffuse reflectivity over 90%, preferably 96% or more. For this purpose, the sheet 150 and the caps 160 may be coated with diffusely reflective tape, such as DRP™ Backlight Reflector (W. L. Gore & Associates), white paint, or more exotic materials such as Labsphere Corporation's Spectrafect paint. The reflectivity of Spectrafect paint is 98%, which is considerably higher than the reflectivity of house paint, which is approximately 92%. DRP™ Backlight Reflector has a reflectivity of approximately 97%-99.5%. Alternatively, the diffusely reflecting sheet 150 and the diffusely reflecting caps 160 may be constructed from a diffusely (or specularly) reflecting material, such as titanium dioxide, pigmented Lexan™ polycarbonate, or Spectralon™ plastic, thereby avoiding the need to apply a separate coating to the sheet 150 and the end caps 160. The reflectivity of Spectralon™ plastic is about 99%. Although it is preferred that the reflective surfaces 150, 160 be diffusively reflective, in an alternative embodiment these surfaces comprise specularly reflecting surfaces that are preferably faceted as in a product sold by 3M under the name Visible Mirror Film (specular or diffuse). Additionally, while the cavity of the preferred embodiment is gas-filled (with air), the cavity may also be formed by a liquid or solid.

Light exits the device 100 through a sheet member or film stack 170, which faces the diffusely reflecting sheet 150. As shown in FIG. 2, the sheet member 170 acts as the output face of the device 100, and comprises an optical conditioning element 210, which may be covered with transmissive outer protective cover 200. The optical conditioning element 210 includes (in the direction of light propagating outward through the sheet member 170) one or more sheets of material, which are substantially parallel to each other, namely, a diffuser 180, an optional first prism sheet 190, and an optional second prism sheet 194. The diffuser 180 acts to randomize the direction of the light incident upon it and preferably has relatively low backscattering. By way of example, the diffuser 180 may be of any construction that will diffuse light, such as translucent sheets of plastic, or plastic with a rough surface. The prism sheets 190 and 194 may each be a brightness-enhancing film (BEF) for reducing the solid angle of the light, with an angular emission in the range of 50 to 80 degrees full width half maximum (FWHM). Brightness-enhancing films suitable for use in the preferred embodiments are commercially available from 3M Corporation. A thin film BEF, having linear pyramidal structures therein, is described in U.S. Pat. No. 5,684,354 to Gleckman, which is hereby incorporated by reference herein. Preferably, the repeated structures of the sheets 190 and 194 are crossed at generally 90 degrees with respect to each other, and are each oriented at 45 degrees with respect to the longitudinal axis of the elongate housing 140.

The diffuser 180 and the prism sheets 190 and 194 of the optical conditioning element 210 spread the light uniformly

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over the output face of the device **100**. The prism sheets also serve to concentrate the optical energy within a field of view, and this causes the light to be directed more intensely in the direction of an observer within that field. While it is preferred that the diffuser **180** be placed below the prism sheets **190** and **194** (as shown in FIG. 2), it will be understood that the position of the diffuser and the prism sheets may be exchanged. The optical conditioning element **210** and the point source **174** are preferably separated by less than 3.5 inches, more preferably by less than 2.5 inches, and still more preferably by less than 1.5 inches. The protective outer cover **200** protects the device **100** from the environment, and may act as a color filter or contain darkened or lightened regions of a specific pattern, such as a logo, design, or alphanumeric characters.

As shown in FIG. 2, the point sources **174**, such as LEDs, are disposed just beneath the optical diverters **110**. Electrical leads (not shown) from the point sources **174** are connected to the printed circuit board **130**, with the sheet **150** having holes punched therein for accepting the leads of the LEDs **174**, such that the sheet is positioned between the LEDs and the printed circuit board. The housing **140** includes lips or flanges **220** for holding the diffusely reflecting sheet **150** in place. The sheet **150** (and the LEDs **174** and the printed circuit board **130** to which the sheet **150** is attached) is advantageously flexible so that it may be slid underneath the lips **220**, permitting the sheet **150** to naturally assume a shape which is typically parabolic in cross section. When the sheet **150** assumes a parabolic cross section, light reflected off the sheet is efficiently directed towards the optical conditioner **210**.

An alternative preferred embodiment is illustrated in FIGS. 3 and 4. In this embodiment, a device **230** includes a cylindrically shaped housing **240** that functions both as a housing and a protective outer cover. The sheet member **170** is secured to a pair of lips or flanges **244** that run along the length of the device **230**. (The flanges **244** may also function the same as the lips **220** of FIG. 2, for holding the reflecting sheet **150** in place.) The device **230** is otherwise substantially similar to its counterpart **100** of FIGS. 1–2, and similar parts are designated with the same reference numerals. The housing **240** may be colored or include darkened portions for producing a desired visual effect. Alternatively, separate elements or layers of film (not shown) disposed between the conditioning element **170** and the housing **240** may be used for achieving a desired optical effect. Such elements may also be used in conjunction with the embodiment shown in FIGS. 1 and 2.

One aspect of the embodiments shown in FIGS. 1–2 and FIGS. 3–4 is that the intensity of light exiting the optical conditioning element **210** is spatially very uniform and thus appears to an observer to have constant luminance across the entire element **210**. This uniformity can be quantified with reference to an imaginary grid of 1 mm² “pixels” on the output side of the optical conditioning element **210**. As used herein, the term “pixel” means any square millimeter cell defined by an imaginary grid on the output side of the element **210** formed by two orthogonal sets of parallel lines separated by 1 mm. Thus, a pixel as used herein does not represent a discrete element, but rather corresponds to a square millimeter of the exterior surface of element **210**. The ratio of the luminance of adjacent pixels is preferably between 0.95 and 1.05, more preferably between 0.98 and 1.02, and still more preferably between 0.99 and 1.01. The ratio of the luminance of non-adjacent pixels is preferably between 0.5 and 2.0, more preferably between 0.57 and 1.75, still more preferably between 0.67 and 1.5, and most

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preferably between 0.77 and 1.3. It will be understood that a given ratio can be more or less than 1.0, depending upon whether the ratio is determined with the intensity of the more intense pixel placed in the numerator or the denominator, respectively.

As illustrated in FIGS. 5A and 5B, the mounting channel **144** is configured to mate with a mounting bracket **250**, such as that illustrated in FIGS. 6A and 6B. The mounting bracket **250** is attached to a plate **260** that may be fastened to a building **270** or other structure using screws **280**, bolts or the like. The mounting bracket **250** may be made of compliant plastic (or another suitable, outdoor-rated material) and comprises a latching member **290**. To secure the mounting bracket **250** to the mounting channel **144**, the profile of the latching member **290** is reduced by pressing the latching member **290** into the mounting channel **144**, thereby squeezing both sides of the latching member about a slot **300**, so that the latching member **290** is received by the mounting channel **144**. Once the latching member **290** is within the channel **144**, it springs back to reassume its uncompressed state (FIG. 6A), thereby holding the lighting device **100** (**230**) in place.

The lighting devices **230** (**100**) may be advantageously constructed in segments of various lengths, such as 2, 4, or 8 feet. Two or more segments may be coupled together by a collar **310** as illustrated in FIGS. 7A and 7B. Within the collar **310** is a dual female connector **320** for receiving respective male connectors **330** from each of two lighting devices **230**. The male connectors **330** are electrically connected to the printed circuit board **130**, and the female connector **320** is tied electrically to a power source via an electrical line **340**. The female connector **320** may be held in place within the collar **310** by, for example, rings or spokes (not shown) that extend within the collar. FIG. 7C shows an alternative arrangement in which power is supplied via a single female connector **360** located at one end of one of the devices **230**. In this case, adjacent devices **230** may be connected by a dual female connector (not shown) to which no electrical line **340** is attached.

A preferred embodiment of the optical diverter **110** is illustrated with respect to FIGS. 8–11. FIG. 8 shows a cross section of an optical diverter **110a** which includes a total internal reflection (TIR) region **400** with a surface **410** that is smoothly curved and defines a vortex shape forming an apex **421** that extends into the optical diverter **110a**. The optical diverter **110a** is surrounded by air, so that a refractive index interface is formed, which permits total internal reflection. The surface **410** of this embodiment substantially completely reflects light incident thereon, such that substantially no light is transmitted therethrough. The TIR region **400** may advantageously have the shape of an equiangular spiral that forms a cusped portion **420**. The surface **410** of FIG. 8 is shown as being axially and circularly symmetrical and extending 360 degrees about a vertical axis **424** aligned with and passing through the point source **174**. However, a TIR diverter (not shown) may be used in which the cusped portion is symmetrical about a line rather than being symmetrically oriented about a point, as in FIG. 8. Such a TIR diverter enjoys planar rather than radial symmetry.

In the embodiment of FIG. 8, the point source **174**, such as an LED, is mounted below the apex **421** of the TIR surface (i.e., just below the point on the cusp **420**) in close proximity thereto, with the reflecting surface extending 360° about the LED and apex. The LED **174** is contained within an LED package **430**, which resides within a recess **440** in the optical diverter **110a**. In order to ensure good coupling into the optical diverters **110** disclosed herein, and to reduce

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reflections at the interface between the LED package 430 and the boundary of the recess 440, a transparent optical coupling agent (not shown), such as an adhesive or gel, may be used to preclude any optically interfering air gaps between the LED 174 and the optical diverter. The transparent optical coupling agent could be an epoxy, silicone, or any well-known organic or inorganic optical coupling material. Preferably, the refractive index of the coupling agent is between that of the LED package and the optical diverter 110.

The surface 410 may be curved, or it may include a plurality of flat surfaces approximating a curve to form a totally internally reflecting (TIR) lens having a focal point. When the point source 174 is positioned (as shown) at this focal point, light generated by the point source 174 is totally internally reflected from the surface 410. If the surface 410 is curved, any one of a number of shapes may be employed, such as a hyperboloid, paraboloid, cone, cusp or other surface of revolution. Mathematical modeling of these shapes can be performed with an optical analysis software package such as ASAP by Breault Research of Tucson, Arizona. The surface 410 is contoured such that substantially all light rays emitted from the LED 174 at the focal point of surface 410 are incident on the surface 410 at an angle at least equal to the critical angle. This may be accomplished by calculating the range of possible incidence angles of light rays from the LED 174 at the focal point at various local portions of the surface 410. The local portions are then oriented so that all rays are incident within the critical range. The local portions could be large in size so that the surface 410 consists of a collection of flat surfaces, for example. As the size of the local portion decreases, the surface 410 forms into a smoothly curved surface having, for example, the equiangular spiral shape shown in FIG. 8.

While a circularly and axially symmetric cusped surface is preferred for many applications, the surface 410 need not be symmetrical. In general, the surface 410 is flared so that light that reflects off of the surface 410 will be directed out of and away from the optical diverter 110a. In this sense, the optical diverter 110a of this embodiment acts as a lateral diverter of light. This flared surface 410 may be viewed as extending between an apex portion of the surface 410 (corresponding to the cusp 420 of FIG. 8) and a base portion 450 above the apex. The base portion 450 flares outwardly (radially) from the vertical axis 424 that passes through the apex 421 and the point source 174. Thus, the flared reflecting surface 410 flares outwardly from the apex 421 to the base portion 450. A groove 480 in the embodiment of FIG. 8 (and the embodiments of FIGS. 9, 10, 11 and 13 discussed below) has a depth such that substantially all rays which would otherwise propagate directly from the point source 174 to the side surface 120 of the diverter 110a are intercepted by at least one wall of the groove. Thus, the groove 480 prevents direct propagation of rays through the side surface 120 and onto the optical conditioning element 210, and thereby prevents such rays from causing non-uniformities in the output luminance.

FIGS. 9–11 depict the optical paths of various rays within the optical diverter 110a, in which FIG. 9 is an overview of the various paths that light rays take. The optical diverter 110a is illustrated as having an annular groove 480, one face of which (surface 490) is frosted. The groove 480 redirects light from the LED 174 that is incident thereon. Light rays emanate from the LED 174 at the focal point of surface 410 within the LED package 430. Some light rays 460 are refracted through the inner side surface of the groove 480 for propagation to the top surface of the groove, where the rays

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460 are again refracted for propagation to the TIR reflecting surface 410. Other rays 470 pass within the region bounded by the inner side surfaces of the groove 480, and thus by-pass the groove for direct propagation to the TIR reflecting surface. Rays 460 and 470 both undergo TIR at surface 410, are reflected downwards, and eventually exit the diverter through side surface 120. As discussed above in connection with FIG. 1, light exiting the diverter 110a is diffusely reflected by the sheet 150 and by the end caps 160 at either end of the device 100 (230), and eventually exits the device through the sheet member 170, which faces the diffusely reflecting sheet 150.

The progress of light rays 460 and 470 through the diverter 110a is shown in more detail in FIGS. 10 and 11, respectively. FIG. 10 shows light rays 460 being refracted by the walls of the groove 480. While some rays 460a pass directly out of the side surface 120 of the diverter 110a after undergoing TIR, other rays 460b are internally reflected towards the frosted surface 490, where they are scattered in many directions before exiting the device 100 (230). FIG. 10 also shows rays 465, which pass through the inner side surface of the groove 480 for propagation to the frosted outer side surface 490, where the rays 465 are scattered in many directions. This scattering prevents them from becoming visible through the output area. FIG. 11 shows light rays 470 undergoing TIR at surface 410 and being refracted at face 120, whereupon the rays 470 exit the diverter 110a. Surface 410 can have a shape tailored to cause uniform illumination of the sheet 150.

Another TIR embodiment is illustrated in FIG. 12, in which an optical diverter 110b includes a flared reflecting surface formed by a cusped portion 492 and a refracting portion formed by an elliptical drum lens or torus portion 494, below the cusped portion 492. Both the cusped portion 492 and the refracting portion 494 are surfaces of revolution about an axis 496 that passes through the point source, 174, as well as through the apex of the cusped portion 492. Light rays 498 that strike surface 410b in the cusped portion 492 undergo total internal reflection and exit the diverter 110b propagating nominally perpendicular to the axis 496. Light rays 500 exiting a surface 502 of the toroidal portion 494 are refracted so that they also propagate nominally perpendicular to the axis 496. Further, the surface 502 is designed so that substantially no rays propagate from the point source 174 through the side surface 120 without first undergoing TIR at surface 410b. The resultant distribution of light outside of the diverter 110b is such that the embodiment of FIG. 12 acts with an isotropic hemispheric source to produce an equatorial distribution with a latitudinal beam width depending on the relative size of the point source 174. The diverter 110b is suitable for use in the lighting devices disclosed herein, but alternatively, it may be used by itself outside of a housing 140 (240) to produce 360 degree, latitudinally narrow output in the far field. Typical applications are aircraft warning beacons for high structures and marine beacon on buoys.

Although the embodiment illustrated in FIGS. 8–11 includes a surface 410 that is totally internally reflecting with respect to light rays 460 and 470, and the embodiment of FIG. 12 also includes a surface 410b that is totally internally reflecting, an alternate embodiment comprises a surface 510 which is only partially rather than totally internally reflecting. As illustrated in FIG. 13, this embodiment includes a flared surface comprising a cusped portion 420c and a base portion 450c. Optical radiation 520 that would otherwise be reflected for propagation through the side face 120 of the optical diverter 110c passes through

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(i.e., is diffusely transmitted by) the surface **510** for propagation directly through the sheet member **170**, without reflecting off the reflective sheet **150** or one of the caps **160**. This may enhance uniformity of illumination of the sheet member **170** and eliminate optical losses associated with reflections off the sheet **150** and the caps **160**. In FIG. 13, however, a substantial portion of the light rays **460** and **470** are preferably still totally internally reflected at surface **510**. The optical diverter **110c** may be advantageously sized to allow at least a substantial portion of the light reflected off the cavity sheet **150** to reach the optical conditioning element **210** without passing through the diverter **110c**, and the reflective surfaces **150** and **160** arranged to allow at least a substantial portion of the light transmitted through the surface **510** to reach the optical conditioning element without reflection. This feature acts to compensate for reduced illumination of the sheet **150** just beneath the diverter **110c**.

A surface **510** that is partially reflecting and partially transmitting may, in general, be formed by appropriately selecting the angle of incidence between the light rays **460** (**470**) and the surface **190**. For example, the surface **510** may be formed at an angle that insures that some light "leaks through" the surface **190** while other light is reflected off of surface **190**. Additionally, the apex of the cusped portion may be rounded to provide controlled leakage of light from the LED **174** through the surface **510** immediately above the LED. This eliminates dark spots above the LED **174**. Moreover, as illustrated in FIG. 13, a surface **410** that is initially totally internally reflecting may be lightly sand-blasted or etched to form distributed scattering centers **530** thereon, such that some of the light incident on the scattering centers passes through the surface **410**. These scattering centers **530** may be distributed non-uniformly on the surface **410**. Also, the surface **410** may be heavily etched or sand-blasted to form a pattern such as a series of concentric rings **540** (see the diverter **110d** of FIG. 14) about a center **544** at an apex of the surface, which likewise results in some of the light leaking through the surface.

The optical diverters shown in FIGS. 8-14 may be comprised of material that is transparent to the light produced by the LED **174**, such as a transparent polymeric material, and may be manufactured by various well-known methods, such as machining or injection molding. Preferred materials for the optical diverters **110** are acrylic, polycarbonate, and silicone. Acrylic, which has an index of refraction of approximately 1.5, is scratch-resistant and has a lower cost relative to polycarbonate. On the other hand, polycarbonate, which has an index of refraction of approximately 1.59, has higher temperature capabilities than acrylic. Polycarbonate also has improved mechanical capabilities over acrylic. Silicone has a refractive index of approximately 1.43. The refractive index of air is nearly 1.0.

While the reflectors of the preferred embodiments are flared, another embodiment (not shown) utilizes a non-flared planar reflector which is partially reflective and partially transmissive. Also, instead of using optical diverters **110** which rely upon total or partial internal reflection, reflection may be provided by partially or totally reflective mirrors (not shown), in which the mirrors are preferably contoured to reflect light laterally. Such mirrors may advantageously include a curved surface, so that light is reflected over a range of angles and scattered within the device **100** (**230**) to provide uniform illumination of the sheet member **170**. This function may also be performed by a transparent optical element that has a non-uniform change in its index of refraction, for example, a gradient index optical element.

The point sources **174** may advantageously comprise an LED cluster that provides tricolor output, e.g., red, green,

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and blue, so that virtually any color may be produced by appropriately selecting the relative intensity of the respective component wavelengths. Further, both gradual and fast time-changes in color are possible, and travelling wave patterns may be generated when the respective outputs of the LEDs **174** are successively varied in a coordinated fashion. Although the point sources **174** have been principally described with respect to LEDs, other point sources may be used, such as miniature incandescent filaments or arc lamps (not shown). However, LEDs are preferred because of their ability to operate at relatively low voltage (e.g., 24 volts DC or less). Also, LEDs generate no RF interference. As a further alternative to using LEDs as the point sources **174**, a fiber optic line (not shown) may be used to distribute light to a series of optical diverters **110**, in which light is tapped off at various points along the fiber optic line (corresponding to the point sources **174**) and is directed into the diverters. In this case, a laser diode or other light generator may be used to couple light into the fiber optic line, and the fibers form the point sources of light.

The cylindrical or semi-cylindrical devices illustrated in FIGS. 1-4 may be used in a number of different applications, such as for decorative illumination, light boxes, backlights, and for guidance along pathways. Further, the housing utilized with the optical diverters **110** and sheet member **170** may be constructed in various sizes and shapes, including wide area planar, linear elongate, and curved elongate. FIG. 15 illustrates one embodiment in which the letter "G" has been formed. Other possible embodiments will be apparent to those skilled in the art. For example, instead of positioning the optical diverters **110** along a line or a curve, the optical diverters may be mounted, for example, in a grid (not shown) to cover a wide-area display, the surface of which may have numbers, letters, logos, or other indicia printed thereon.

It should be understood that the scope of the present invention is not limited by the illustrations or the foregoing description thereof, and that certain variations and modifications of the foregoing embodiments will suggest themselves to one of ordinary skill in the art.

What is claimed is:

1. An illumination apparatus, comprising:

a cavity having reflective surfaces and an output area; at least one light source disposed in said cavity, said light source comprising a point source and an optical diverter having a flared reflecting surface; and an optical conditioning element over said output area, said optical conditioning element comprising at least a diffuser.

2. The apparatus of claim 1, wherein said flared reflecting surface extends between an apex portion of said surface and a base portion of said surface, said diverter having an axis passing through the apex portion and the point source, said base portion being above the apex portion and extending radially outwardly from said axis such that the reflecting surface flares outwardly from the apex portion to the base portion.

3. The apparatus of claim 2, wherein the flared surface is curved.

4. The apparatus of claim 3, wherein the flared surface is cusped.

5. The apparatus of claim 2, wherein the flared surface is formed by a refractive index interface configured to totally internally reflect light from the point source laterally outwardly from said axis.

6. The apparatus of claim 1, wherein the point source comprises an LED.

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7. The apparatus of claim 1 wherein the point source comprises a miniature incandescent filament or arc lamp.

8. The apparatus of claim 1, wherein the optical conditioning element comprises a prism sheet.

9. The apparatus of claim 8, additionally comprising a second prism sheet, each prism sheet having repeated structures oriented generally orthogonal to repeated structures of the other prism sheet.

10. The apparatus of claim 8, wherein the prism sheet and diffuser are in substantially parallel relationship, with the diffuser closer to the light sources than the prism sheet.

11. The apparatus of claim 1, wherein said cavity is within an elongate housing having a width which is not substantially greater than the width of the output area.

12. The apparatus of claim 11, wherein the optical conditioning element comprises at least one prism sheet having repeated structures oriented at about 45° relative to a longitudinal axis of the elongate housing.

13. The apparatus of claim 11, wherein the apparatus comprises at least two of said elongated housings coupled end to end.

14. The apparatus of claim 1, wherein the point source and the optical conditioning element are separated by 3½ inches or less.

15. The apparatus of claim 1, wherein the point source and the optical conditioning element are separated by 2½ inches or less.

16. The apparatus of claim 1, wherein the point source and the optical conditioning element are separated by 1½ inches or less.

17. The apparatus of claim 1, wherein the cavity reflecting surfaces are diffusively reflective.

18. The apparatus of claim 17, wherein the diffusively reflective surfaces have a reflectivity of at least 90%.

19. The apparatus of claim 1, wherein the flared reflecting surface is partially reflective and partially transmissive.

20. An illumination apparatus, comprising:

a housing comprising a cavity having reflective surfaces and an output aperture;

an optical conditioning element across the output aperture, said conditioning element comprising at least one sheet having a plurality of pixels;

at least one light source disposed within said cavity directly beneath said conditioning element, said at least one light source comprising a point source spaced less than 3½ inches from said sheet and illuminating said reflective surfaces such that the ratio of the luminance of adjacent pixels is between 0.95 and 1.05 and the ratio of the luminance of non-adjacent pixels is between 0.5 and 2.0, whereby the appearance of illumination at said sheet is substantially uniform.

21. The apparatus of claim 20, wherein said reflective surfaces of said cavity are diffusively reflective with a reflectivity of at least 90%.

22. The apparatus of claim 20, wherein said ratio of adjacent pixels is 0.98 to 1.02.

23. The apparatus of claim 20, wherein said ratio of adjacent pixels is 0.99 to 1.01.

24. The apparatus of claim 20, wherein said ratio of non-adjacent pixels is 0.57 to 1.75.

25. The apparatus of claim 20, wherein said ratio of non-adjacent pixels is 0.67 to 1.5.

26. The apparatus of claim 20, wherein said ratio of non-adjacent pixels is 0.77 to 1.3.

27. The apparatus of claim 20, wherein said sheet comprises a prism sheet.

28. The apparatus of claim 27, wherein the optical conditioning element comprises a diffuser sheet disposed below the prism sheet.

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29. The apparatus of claim 28, wherein the optical conditioning element comprises a second prism sheet.

30. The apparatus of claim 20, wherein said at least one light source comprises a point source and a total internal reflection lens having a cusped surface for reflecting light from the point source against said diffusive reflective surfaces.

31. The apparatus of claim 20, wherein the apparatus has plural light sources spaced by 2½ inches or less from the sheet.

32. The apparatus of claim 20, wherein the apparatus has plural light sources spaced from each other by at least one-half inch.

33. An illumination apparatus, comprising:

a cavity formed by reflective material, said cavity having an output area;

an optical conditioning element at said output area;

a light source in said cavity, said light source comprising a point source and an optical diverter having a reflecting surface that is partially reflective and partially transmissive, said reflective surface allowing a portion of light incident thereon to pass through the reflecting surface, while reflecting another portion of the incident light onto the reflective material, said reflective material reflecting light within said cavity, whereby said output area and optical conditioning element are illuminated.

34. The apparatus of claim 33, wherein said reflective material is diffusively reflective with a reflectivity of at least 90%.

35. The apparatus of claim 33, wherein said reflecting surface of said optical diverter is comprised of a refractive index interface that totally internally reflects said substantial portion of the incident light while permitting another portion of light to pass through the interface.

36. The apparatus of claim 35, wherein said reflecting surface of said optical diverter is comprised of scattering centers that scatter light incident thereon.

37. The apparatus of claim 36, wherein the scattering centers are distributed over said reflecting surface.

38. The apparatus of claim 37, wherein the distribution is non-uniform.

39. The apparatus of claim 38, wherein the scattering centers are in the form of a pattern.

40. The apparatus of claim 39, wherein the pattern comprises concentric rings having a center at a vertex of the reflective surface.

41. An illumination apparatus, comprising:

an optical diverter comprised of transparent material having a reflecting surface formed by a refractive index interface configured to totally internally reflect light from a point source positioned to emit a first portion of light rays towards the reflecting surface and a second portion of light rays towards a side surface of the diverter, said diverter comprising a refracting interface that refracts the second portion of light rays towards the reflecting surface, such that both the first and second portions of light rays are reflected from said reflecting surface.

42. The illumination device of claim 41, wherein said point source emits a third portion of light rays towards said side surface, said diverter further comprising a scattering surface that scatters said third portion of rays.

43. The illumination device of claim 41, wherein the point source is disposed at the bottom of the diverter, and the reflecting surface is oriented to reflect the first and second portions of light rays towards the bottom of the diverter.

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44. An illumination apparatus, comprising:
an optical diverter comprised of transparent material
having a flared reflecting surface formed by a refractive
index interface, said interface configured to totally
internally reflect light from a point source that is
positioned adjacent to an apex of the flared reflecting
surface and which emits light rays for reflection by the
reflecting surface. 5
45. The apparatus of claim 44, wherein at least a portion
of the reflecting surface is partially transmissive such that
some of the light is transmitted through the surface. 10
46. The apparatus of claim 45, wherein said portion
comprises the apex.
47. The apparatus of claim 44, wherein the reflective
surface substantially completely reflects light incident
thereon, such that substantially no light is transmitted there-
through. 15
48. The apparatus of claim 44, wherein the reflecting
surface extends 360° about the apex.
49. The apparatus of claim 44, comprising a drum lens 20
forming an integral portion of the diverter.
50. An illumination apparatus, comprising:
a cavity having reflective surfaces and an output area;
at least one light source disposed in said cavity, said light
source comprising a point source and an optical

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- diverter having a surface that is partially reflective and
partially transmissive;
- an optical conditioning element over said output area, said
optical conditioning element comprising a diffuser, said
diverter positioned between the point source and opti-
cal conditioning element such that (a) a portion of light
emitted by the point source is reflected from the
diverter towards the reflective surfaces of the cavity,
and (b) another portion of light emitted by the point
source is transmitted through the surface of the diverter
towards the optical conditioning element, said diverter
sized to allow at least a substantial portion of the
reflected light to reach the optical conditioning element
without passing through the diverter, said diverter and
said reflective surfaces of said cavity arranged to allow
at least a substantial portion of the transmitted light to
reach the optical conditioning element without under-
going reflection.
51. The illumination apparatus of claim 50, wherein the
diverter comprises a lateral diverter.
52. The illumination apparatus of claim 51, wherein the
lateral diverter has a flared surface.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,582,103 B1
DATED : June 24, 2003
INVENTOR(S) : Popovich et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3,

Line 47, delete "s plural" and insert -- plural -- therefor.

Line 49, after "(LED)" insert -- 174 --.

Column 4,

Line 13, before "surfaces" insert -- The --. (begins new paragraph)

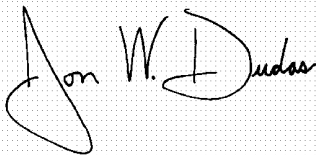
Column 8,

Line 36, delete "source, 174" and insert -- source 174 -- therefor.

Line 60, delete "hat" and insert -- that -- therefor.

Signed and Sealed this

Tenth Day of May, 2005

A handwritten signature in black ink on a light gray grid background. The signature is written in a cursive, stylized font and appears to read "Jon W. Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office

EXHIBIT W-4

(12) **United States Patent**
Yoshizoe

(10) **Patent No.:** US 6,674,507 B2
(45) **Date of Patent:** Jan. 6, 2004

(54) **METHOD FOR MANUFACTURING FLAT TYPE DISPLAY INCLUDES FORMING CLOSED LOOP CONSISTING OF SEALANT WITH RECESS FORMED INSIDE THE LOOP**

(58) **Field of Search** 349/153, 189, 349/190

(75) **Inventor:** Hidefumi Yoshizoe, Izumi (JP)

(73) **Assignees:** NEC Corporation (JP); NEC LCD Technologies, Ltd. (JP)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 13 days.

(21) **Appl. No.:** 10/156,904

(22) **Filed:** May 29, 2002

(65) **Prior Publication Data**

US 2003/0025867 A1 Feb. 6, 2003

(30) **Foreign Application Priority Data**

Aug. 2, 2001 (JP) 2001-234935

(51) **Int. Cl.⁷** G02F 1/1339

(52) **U.S. Cl.** 349/190; 349/153

(56) **References Cited**

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* cited by examiner

Primary Examiner—Tarifur R. Chowdhury

(74) *Attorney, Agent, or Firm*—Hayes Soloway P.C.

(57) **ABSTRACT**

A belt-shaped sealant is coated on a substrate to surround a periphery of a display region of a flat type display device. A start point and a termination point of the sealant are disposed remote from the display region such that the sealant never intrudes into the inside of the display region when the sealant is pressed between opposing substrates of the display device.

5 Claims, 4 Drawing Sheets

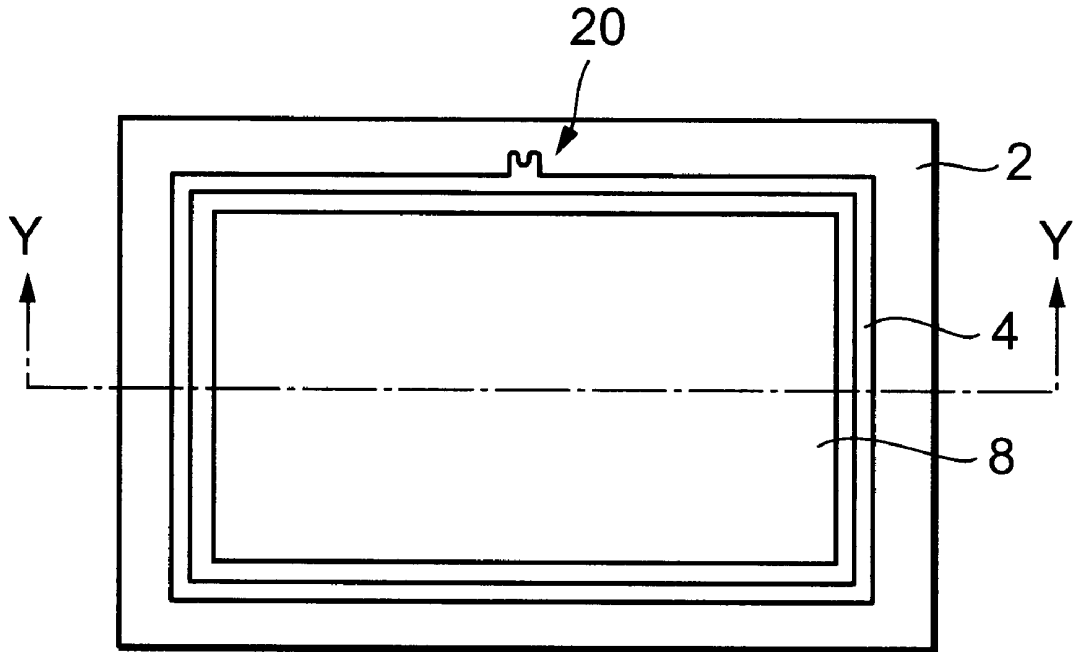


FIG.1 (PRIOR ART)

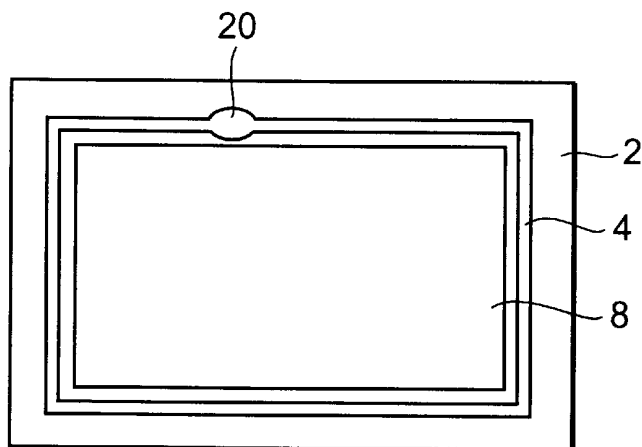


FIG.2 (PRIOR ART)

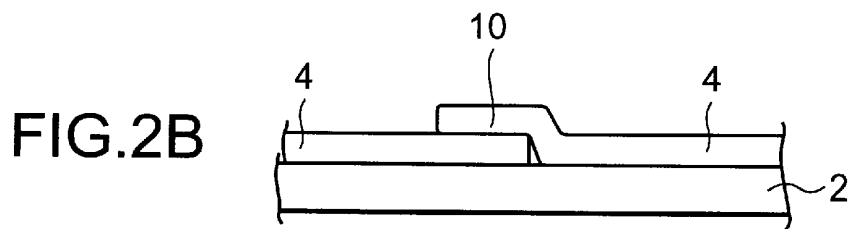
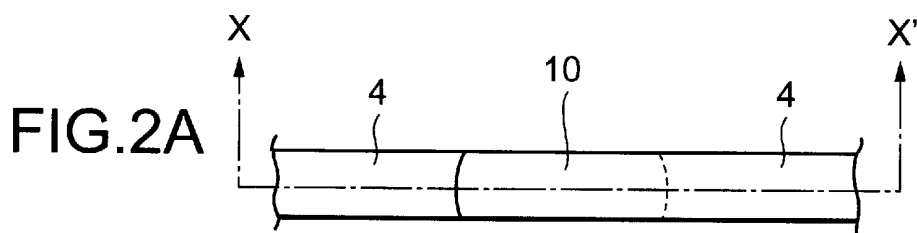


FIG.3

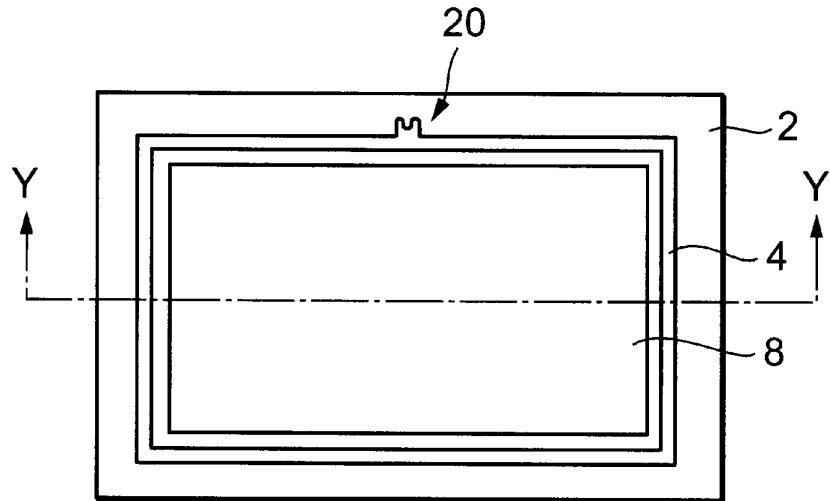


FIG.4

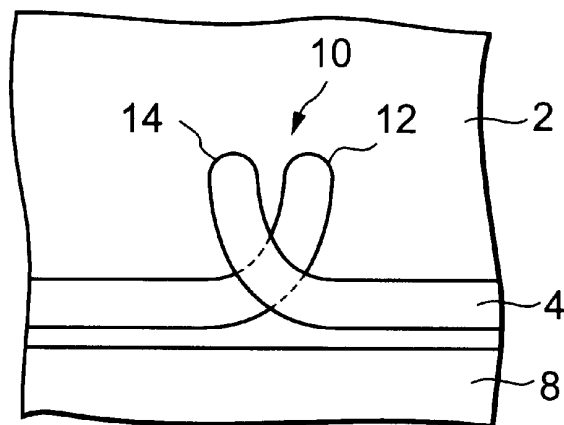


FIG.5

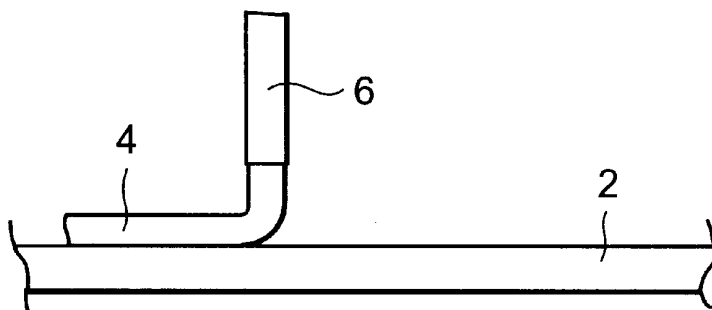


FIG.6

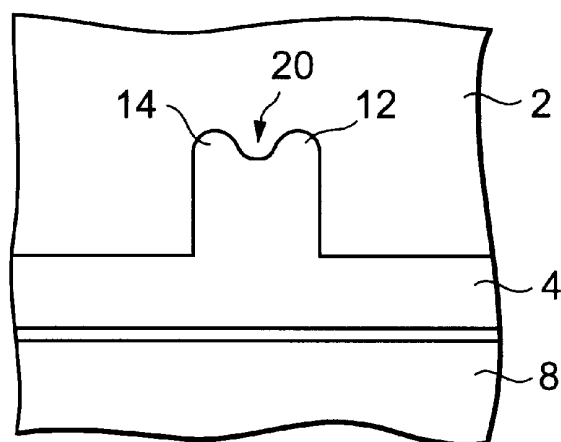


FIG.7

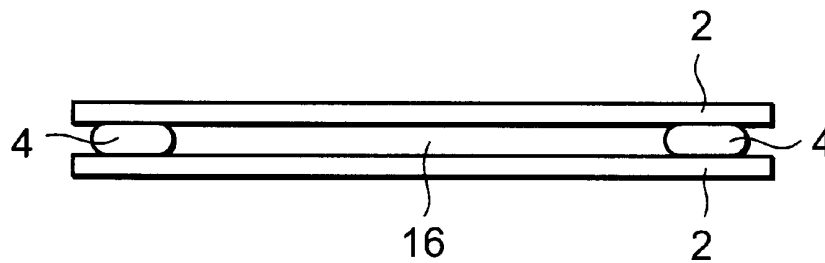
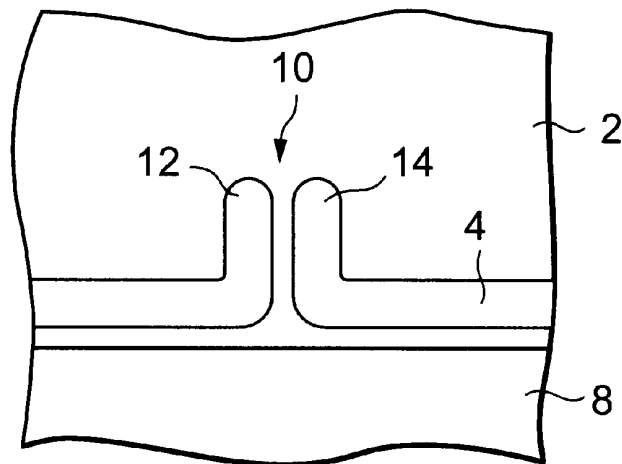


FIG.8



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**METHOD FOR MANUFACTURING FLAT
TYPE DISPLAY INCLUDES FORMING
CLOSED LOOP CONSISTING OF SEALANT
WITH RECESS FORMED INSIDE THE LOOP**

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for manufacturing a flat type display device and a flat type display device manufactured by the same, and particularly to a sealant applying method, which is used for sealing a liquid crystal material within a liquid crystal panel.

2. Description of the Prior Art

Conventionally, the following methods as a method for sealing a liquid crystal within the inside of a liquid crystal panel have been known. That is, in one case, a sealant is applied to one substrate to form an closed loop thereon and the one substrate is adhered to the other substrate via the closed-loop-shaped sealant, and then, a liquid crystal material is sucked into a space between the one and other substrates via a gap formed in via the closed-loop-shaped sealant. In another case, a sealant is applied to one substrate to form an closed loop thereon and a liquid crystal material is dropped within the closed loop on the one substrate, and then, the other substrate is adhered to the one substrate having the liquid crystal material dropped thereon via the closed-loop-shaped sealant.

According to the one method in which a liquid crystal is sucked into a space between the one and other substrates, it is necessary to keep a part of the sealant open so that the part serves as an inlet through which a liquid crystal material is guided into the space between the two substrates. According to the other method in which a liquid crystal material is dropped on one substrate, as shown in a plan view of FIG. 1, a sealant 4 is coated on a substrate 2 so as to completely surround a periphery of a display region 8. Therefore, when using a nozzle to coat a sealant, the sealant 4 is coated such that one end portion of the sealant 4 overlaps the other end portion thereof at around a start point where the sealant begins traveling on the substrate and a termination point where the sealant terminates traveling on the substrate, as shown in FIGS. 2A and 2B. Note that FIG. 2A is an enlarged plan view of an overlapped portion 10 in a situation where the sealant is coated on the substrate 2 such that one end portion of the sealant overlaps the other end portion thereof and the substrate 2 and the other substrate are disposed facing each other before pressing the two substrates to adhere to each other. FIG. 2B is a sectional view of the overlapped portion 10 cut along the line X-X' of FIG. 2A.

However, as described above, when the sealant 4 is coated on the substrate 2 such that one end portion of the sealant overlaps the other end thereof and the substrate 2 and the other substrate are pressed against each other, the overlapped portion 10 becomes wider than other portion of the sealant in which the sealant is not made overlapped each other while intruding into the display region 8, as shown in FIG. 1, thereby causing various problems. To prevent the sealant, i.e., an expanded-overlapped portion 20, from intruding the display region, the overlapped portion 10 has to previously be formed apart a long distance from the display region 8, thereby forcing a manufacturer to keep an additional space for a sealant.

SUMMARY OF THE INVENTION

An object of this invention is to provide a method for manufacturing a flat type display device to prevent a sealant

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from intruding into a display region of the device and remove an undesired space from the device by reducing spacing between the sealant and the display region. Another object of this invention is to provide a flat type display device manufactured by the above-described method.

The method for manufacturing a flat type display device according to the present invention is constructed such that a sealant is coated on at least one of two opposing substrates so as to surround a display region in such a manner that a start point and a termination point of the sealant are displaced from the display region toward a periphery of the at least one of two opposing substrates, the start point and termination point being defined such that coating of the sealant begins at the start point and terminates at the termination point, and the two opposing substrates are adhered to each other to form a closed loop consisting of the sealant with a recess formed in an inner periphery of the closed loop.

The method for manufacturing a flat type display device has two application forms as follows.

First, the sealant is coated to cross over a part of the sealant before the termination point, the part being located just next to the start point.

Secondly, the start point and the termination point are apart from each other before the step for adhering the two opposing substrates to each other and the start point and the termination point of the sealant melt in each other in the step for adhering the two opposing substrates to each other.

Therefore, according to a method for manufacturing a flat type display device constructed in accordance with the present invention, when coating a sealant on a periphery of a display region of a flat type display device, the sealant is coated such that the sealant is formed traveling apart gradually from the display region toward start and termination points of the sealant while overlapping a part thereof outside the closed loop portion and therefore, even when the two substrates are adhered to each other to resultantly widen the width of the sealant, the sealant never intrudes into the display region.

BRIEF DESCRIPTION OF THE INVENTION

FIG. 1 is a plan view of a conventional liquid crystal display device to show how a sealant loop looks like when two substrates are apposed together by bonding.

FIG. 2A is an enlarged plan view of the overlapped portion of a sealant loop of the conventional liquid crystal display device before the two substrates are apposed together by bonding. FIG. 2B is a sectional view of the same overlapped portion cut along the line X-X' of FIG. 2A.

FIG. 3 is a plan view of a liquid crystal display device representing a first example of this invention to show how a sealant loop looks like when two substrates are apposed together by bonding.

FIG. 4 is an enlarged plan view of the overlapped portion of the sealant loop of the liquid crystal display device representing the first example of this invention, before the two substrates are apposed together by bonding. FIG. 4 puts a focus on the overlapped portion of the sealant loop formed in accordance with this invention.

FIG. 5 is a diagram to show how a nozzle looks like when it ejects a sealant thread for application.

FIG. 6 is a plan view of the liquid crystal display device representing the first example of this invention to show how the sealant loop looks like when the two substrates are apposed together by bonding.

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FIG. 7 is a sectional view of the liquid crystal display device of the first example cut along the line Y-Y' of FIG. 3.

FIG. 8 is an enlarged plan view of closely apposed both ends of a sealant loop of a liquid crystal display device representing a second example of this invention, before two substrates are apposed together by bonding.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of a method for manufacturing a flat type display device and a flat type display device manufactured through the method, both being constructed in accordance with the present invention and the flat type display device being exemplified by a liquid crystal display device, will be described below.

FIG. 3 is a plan view of a sealant 4 in a situation where one substrate having the sealant 4 coated thereon is adhered to the other substrate via the sealant 4. As can be seen in the figure, the sealant 4 is securely coated on a predetermined portion (shaped like a closed loop) of the substrate 2. The two substrates are adhered to each other in the following manner

FIG. 4 is an enlarged plan view of an overlapped portion 10 of a sealant 4. As shown in FIG. 4, a portion apart from a predetermined portion (closed loop portion) on which a sealant should be coated is determined as a start point 12 and then, coating of the sealant 4 begins at the start point 12 by using a nozzle. The start point 12 is a portion on which the sealant is coated, in more detail, externally spaced a predetermined distance from the display region 8. The sealant 4 is coated starting from the start point 12 while traveling to the predetermined portion (closed loop portion) in an arc form. When the nozzle reaches the predetermined portion (closed loop portion) on which the sealant should be coated, the sealant changes its direction of travel and thereafter, is coated traveling sequentially along the predetermined portion (closed loop portion). Note that the sealant 4 is coated on the substrate 2 using a nozzle 6 shown in FIG. 5.

In this case, two coating methods can be available.

That is, the sealant 4 is coated on the substrate 2 by moving the nozzle 6 itself or contrary to it, by moving the substrate 2 with respect to the nozzle 6. The predetermined portion on which the sealant should be coated is defined as a periphery of the display region 8, i.e., a portion (closed loop portion) along an outer periphery of the region in which a liquid crystal is enclosed.

When the sealant 4 has traveled along and entirely around the predetermined portion (closed loop portion), the nozzle 6 makes the sealant 4 change its direction of travel at a position where the sealant crosses over the portion of the sealant extending from the closed loop portion toward the start point 12 and then, the sealant is coated traveling toward the termination point 14. Thereafter, when the sealant has been coated reaching a position equivalent to the start point 12 with respect to the closed loop portion, the nozzle 6 is stopped to complete the coating. The position is defined as the termination point 14.

After the sealant is coated on the substrate 2, the following process steps are carried out: disperse spacers (not shown) within the display region 8 or drop a predetermined amount of liquid crystal material on the display region 8; and dispose the two substrates so as to face each other; and then, apply a predetermined pressure at a specific temperature to adhere the two substrates to each other. As can be seen in FIG. 3, the sealant 4 is securely coated on the predetermined portion.

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How a geometric shape of the overlapped portion 10 of the sealant 4 before the two substrates are adhered to each other looks like after the two substrates have been adhered to each other is shown in FIG. 6. As already described, the sealant 4 on the substrate before two substrates are adhered to each other is disposed on the substrate such that the sealant begins to travel from the position externally spaced from the predetermined portion (the portion surrounding the display region in a rectangular form) on which the sealant should be coated and then, travels along the predetermined portion, and thereafter, returns to around the start point 12 while being apart from the predetermined portion. In this case, although the two end portions of the sealant 4 are overlapped each other around a portion where the sealant returns to around the start point 12, the overlapped portion of the sealant is located on a position outside the display region 8 (refer to FIG. 4). Accordingly, even when the other substrate is adhered to the substrate 2 to resultantly widen the width of the overlapped portion 10 of the sealant 4 after completion of process steps such as dispersion of spacers and dropping of liquid crystal material, since the overlapped portion 10 is positioned outside the predetermined portion, the widened overlapped portion 20 never affects the display region. As described above, the method for coating a sealant according to the present invention can be summarized as follows.

That is, a method for manufacturing a display device comprises:

- a step for coating at least one string of a sealant on a first substrate forming a closed loop of the sealant so that the sealant begins to travel from one end of the sealant, the one end located outside the closed loop, and then, along the closed loop until the sealant comes within a predetermined distance of the one end, and further, approaches the one end while gradually being apart from the closed loop to finally stop its travel spaced a distance shorter than a specific value from the one end;
- a step for dropping a liquid crystal material inside the closed loop of the sealant on the first substrate; and
- a step for adhering a second substrate to the sealant on the first substrate.

A first aspect of the method for coating a sealant of the present invention is constructed such that in the above-described method for coating a sealant, the sealant travels crossing over the sealant already coated on the first substrate before the sealant finally stops its travel.

A second aspect of the method for coating a sealant of the present invention is constructed such that in the above-described method for coating a sealant, two adjacent ends of the sealant are disposed apart from each other and in the step for adhering the second substrate to the sealant on the first substrate, the two adjacent ends melt in one another and the melted portion of the sealant never intrudes into the region inside the closed loop.

Furthermore, as shown in FIG. 4, the sealant is coated drawing an arc toward the start point 12 and the termination point 14, respectively, and the overlapped portion of the sealant is positioned outside the predetermined portion (closed loop portion). Accordingly, even when the overlapped portion 10 of the sealant 4 of FIG. 4 is pressed to resultantly widen the width of the overlapped portion, the sealant 4 never intrudes into the display region 8. Note that the arc of the sealant 4 and the position of the overlapped portion are appropriately adjusted not to make the sealant intrude into the display region depending on the degree of spread of the sealant 4 observed when the sealant is pressed.

The liquid crystal display device formed as described above presents a cross sectional view thereof as shown in

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FIG. 7. Note that FIG. 7 is a cross sectional view taken along a line Y-Y' of FIG. 3. As shown in FIG. 7, the sealant 4 is provided between the two substrate having such components as an electrode and a color filter therein and a liquid crystal material 16 is enclosed within a closed space sealed by the sealant and the two substrates, and then, a polarizer (not shown) or the like is provided on the associated portion, and finally, electrodes (not shown) on the two substrates are supplied with electricity to display images.

A method for coating a sealant of another embodiment of the present invention is shown in FIG. 8. Although the sealant 4 of FIG. 4 is formed to make one end portion thereof cross over the other end portion thereof outside the closed loop portion, the sealant of this embodiment is formed such that two end portions of the sealant are apart from each other as shown in FIG. 8. Also in the embodiment, the two end portions of the sealant 4 melt in one another after curing of the sealant to enclose the periphery of the display region 8 by the sealant.

It will be appreciated that although the embodiments are described to form only one liquid crystal display device on the substrate 2, the embodiments can be applied to a case where a plurality of liquid crystal display devices are formed on the substrate 2. Furthermore, the closed loop portion of the sealant 4 of the embodiments is not necessarily required to present a rectangular geometric shape. In addition, the position of the overlapped portion 10 is not necessarily required to be located in the center of a side of the closed loop portion of the sealant 4 and may be located at other positions such as a corner of the closed loop portion. Moreover, needless to say that the present invention is not limited to the liquid crystal display device described in the embodiments and may be applied to other display devices that are formed by adhering two substrates to each other.

As described so far, according to a method for manufacturing a flat type display device and a flat type display device manufactured by the method, both being constructed in accordance with the present invention, when coating a sealant on periphery of a display region of a flat type display device, the sealant is coated such that the sealant is formed traveling apart gradually from the display region toward start and termination points of the sealant and therefore, even when the two substrates are adhered to each other to resultantly widen the width of the sealant, the sealant never intrudes into the display region.

What is claimed is:

1. A method for manufacturing a flat type display device comprising the steps of:

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coating a sealant on at least one of two opposing substrates so as to surround a display region in such a manner that a start point and a termination point of said sealant are displaced from said display region toward a periphery of said at least one of two opposing substrates, said start point and termination point being defined such that coating of said sealant begins at said start point and terminates at said termination point; and adhering said two opposing substrates to each other to form a closed loop consisting of said sealant with a recess formed in an inner periphery of said closed loop.

2. The method for manufacturing a flat type display device according to claim 1, wherein said start point and said termination point are apart from each other before said step for adhering said two opposing substrates to each other and said start point and said termination point of said sealant melt in each other in said step for adhering said two opposing substrates to each other.

3. The method for manufacturing a flat type display device according to claim 1, wherein said sealant is coated so as to form a cross-over portion adjacent to said termination point and said start point.

4. The flat type display device manufactured by using the method for manufacturing a flat type display device of claim 1.

5. A method for manufacturing a flat type display device comprising the steps of:

coating a sealant having a constant width on at least one of two opposing substrates so as to dispose said sealant on a portion of said at least one of two opposing substrates apart a predetermined distance from a periphery of said at least one of two opposing substrates; and

adhering said two opposing substrates to each other to form a closed loop consisting of said sealant,

said method being further constructed such that a start point and a termination point of said sealant are displaced from said closed loop toward a periphery of said at least one of two opposing substrates so as not to form a projection intruding into an inner periphery of said closed loop, said start point and termination point being defined such that coating of said sealant begins at said start point and terminates at said termination point.

* * * * *

EXHIBIT W-5

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Hsu *et al.*

Serial No.: 10/921,508

Filed: August 19, 2004

Confirmation No.: 9818

Group Art Unit: 2871

Examiner: Nguyen, Thanh-Nhan P.

TKHR Ref: 250330.1010

Client Ref: 92268US

For: **LIQUID CRYSTAL DISPLAY CELL AND METHOD FOR MANUFACTURING
THE SAME**

AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

The non-final Office Action dated December 19, 2006 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

Application Serial No. 10/921,508
Art Unit 2871

AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("___") and the language being deleted contains a strikethrough ("—").

LISTING OF CLAIMS

1. (Previously Presented) A method for manufacturing a liquid crystal display cell comprising the following steps:

forming a sealing member having a main portion enclosing a display region and a protrusion part extending from the main portion wherein the sealing member is formed by the following steps:

applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and

continuing applying the sealing material along the display region to form the main portion of the sealing member, wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region;

dispensing a liquid crystal material upon one of the pair of substrates;

superposing one of the pair of substrates upon the other one such that the liquid crystal material is enclosed by the sealing member;

curing the sealing member;

cutting the pair of substrates to obtain the liquid crystal display cell.

Application Serial No. 10/921,508
Art Unit 2871

2. (Original) The method for manufacturing a liquid crystal display cell according to claim 1, wherein the sealing material is a radiation-curable adhesive.

3. (Original) The method for manufacturing a liquid crystal display cell according to claim 1, wherein one of the pair of substrates has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

4. (Original) The method for manufacturing a liquid crystal display cell according to claim 1, wherein the cutting step proceeds along a cutting line of the pair of substrates, and the cutting line is across the protrusion part of the sealing member.

*Application Serial No. 10/921,508
Art Unit 2871*

5. (Previously Presented) A liquid crystal display cell comprising:

a first substrate;

a second substrate;

a liquid crystal layer sandwiched between the first substrate and the second substrate; and

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and a protrusion part extending from the main portion and the sealing member is formed by the following steps:

applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and

continuing applying the sealing material along the display region to form the main portion of the sealing member after forming the protrusion part, wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region.

6. (Original) The liquid crystal display cell according to claim 5, wherein the sealing material is a radiation-curable adhesive.

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Art Unit 2871*

7. (Original) The liquid crystal display cell according to claim 5, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

8. (Previously Presented) A liquid crystal display device including at least a backlight module and a liquid crystal display cell, wherein the liquid crystal display cell comprises:

a first substrate;

a second substrate;

a liquid crystal layer sandwiched between the first substrate and the second substrate; and

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and a protrusion part extending from the main portion and the sealing member is formed by the following steps:

applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and

continuing applying the sealing material along the display region to form the main portion of the sealing member after forming the protrusion part, wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region.

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Art Unit 2871

9. (Original) The liquid crystal display device according to claim 8, wherein the sealing material is a radiation-curable adhesive.

10. (Original) The liquid crystal display device according to claim 8, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

11. (Currently Amended) A liquid crystal display cell comprising:

a first substrate;

a second substrate;

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and only a protrusion part extending from the main portion, wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region; and

a liquid crystal layer sandwiched between the first substrate and the second substrate and formed within the display region enclosed by the main portion of the sealing member.

12. (Original) The liquid crystal display cell according to claim 11, wherein the main portion has at least four side walls.

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Art Unit 2871

13. (Original) The liquid crystal display cell according to claim 12, wherein the main portion is rectangular in shape.

14. (Original) The liquid crystal display cell according to claim 11, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

15. (Currently Amended) A liquid crystal display device including at least a backlight module and a liquid crystal display cell, wherein the liquid crystal display cell comprises:

a first substrate;

a second substrate;

a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and only a protrusion part extending from the main portion, wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region; and

a liquid crystal layer sandwiched between the first substrate and the second substrate and formed within the display region enclosed by the main portion of the sealing member.

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Art Unit 2871*

16. (Original) The liquid crystal display device according to claim 15, wherein the first substrate has a light-shielding matrix, and the sealing member is not overlapped with a vertical projected area of the light-shielding matrix.

17. (Original) The liquid crystal display device according to claim 15, wherein the main portion has at least four side walls.

18. (Original) The liquid crystal display device according to claim 17, wherein the main portion is rectangular in shape.

19. (Previously Presented) The liquid crystal display device according to claim 15, wherein the width of the protrusion part is substantially the same width as the main portion enclosing the display region.

Application Serial No. 10/921,508
Art Unit 2871

REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed December 19, 2006. The Examiner is thanked for the thorough examination of the present application. Upon entry of this response, claims 1-19 are pending in the present application. Claims 1-10 are rejected under 35 U.S.C. §112, 2nd paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 5, 11-13, and 19 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by *Yoshizoe* (U.S. Pat. No. 6,674,507). Furthermore, claims 2-4, 6, 7, and 14 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Yoshizoe* in view of Admission (Prior Art). Finally, claims 8-10 and 15-18 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Yoshizoe*, in view of Admission (Prior Art), further in view of *Suzuki* (U.S. Pub. No. 2002/0012094).

Applicants have amended independent claims 11 and 15 and respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

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I. Response to Claim Rejections Under 35 U.S.C. § 112

The Office Action states on page 2 that claims 1-10 are rejected under 35 U.S.C. §112, 2nd paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Office Action refers to the feature in independent claims 1, 5, 8 which recites, "wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region."

The Examiner states that the terms "initial end" and "opening area" [sic] are unclear as claimed. (Applicants assume that Examiner meant "overlapping area" rather than "opening area" since these terms were emphasized in the Office Action on page 2.) To aid the Examiner in understanding this feature, Applicants refer to FIG. 3 from the specification as shown below:

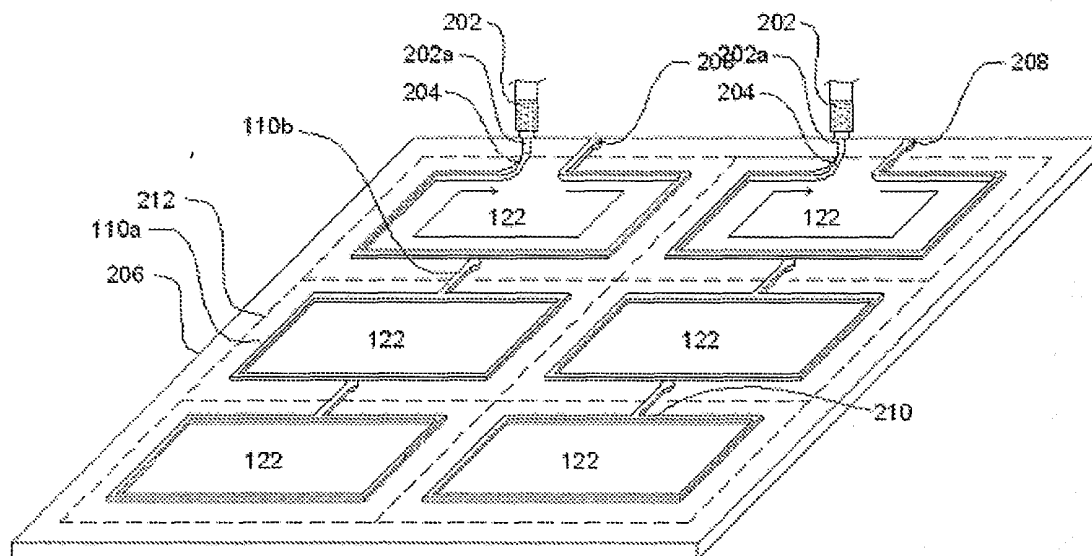


FIG. 3

The "initial end" recited in the claims refers to end (208) shown in the figure. Furthermore, the "overlapping area" refers to area (210) shown in the figure. As clearly illustrated in FIG. 3 above, the initial end and the overlapping area are different. Furthermore, the overlapping area extends along one side of the display region (e.g., the top side of display region (122) above). Therefore, Applicants submit that the feature, "wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region," is not indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Accordingly, Applicants respectfully request that the §112 rejection of claims 1-10 be withdrawn.

II. Response to Claim Rejections Under 35 U.S.C. § 102

Claims 1, 5, 11-13, and 19 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by *Yoshizoe*. For at least the reasons set forth below, Applicants traverse these rejections.

Independent Claim 1 is Patentable Over Yoshizoe

Applicants respectfully submit that independent claim 1 patentably defines over *Yoshizoe* for at least the reason that *Yoshizoe* fails to disclose, teach or suggest certain features in claim 1.

Claim 1 recites:

1. A method for manufacturing a liquid crystal display cell comprising the following steps:

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forming a sealing member having a main portion enclosing a display region and a protrusion part extending from the main portion wherein the sealing member is formed by the following steps:

applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and

continuing applying the sealing material along the display region to form the main portion of the sealing member, **wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region;**

dispensing a liquid crystal material upon one of the pair of substrates;

superposing one of the pair of substrates upon the other one such that the liquid crystal material is enclosed by the sealing member;

curing the sealing member;

cutting the pair of substrates to obtain the liquid crystal display cell.

(*Emphasis added.*) The Office Action alleges that the *Yoshizoe* reference teaches all the features of claim 1. However, the Office Action completely fails to take into consideration the feature emphasized in claim 1 above ("wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region"). Applicants submit that in light of the arguments made in response to the §112 rejection above, this feature should not be excluded from claims 1-10. (The Office Action states on page 2 that "for the examination purpose, claims 1-10 will be interpreted as excluded the limitation above.")

Even assuming, *arguendo*, that the Office Action had included this feature in its rejection, Applicants submit that the *Yoshizoe* reference does not teach this feature. Applicants refer to FIGS. 4 and 8 of the *Yoshizoe* reference, which illustrate the overlapped portions of a sealant loop formed in accordance with the invention of *Yoshizoe*.

FIG. 4

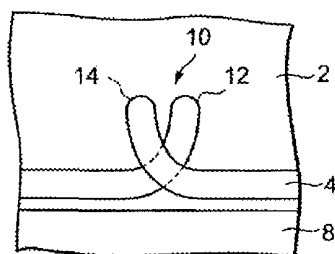
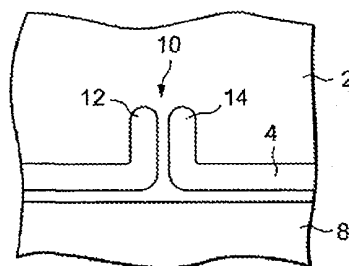


FIG. 8



As seen in the figures above, the *Yoshizoe* reference does not teach the feature, “wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region,” as illustrated in FIG. 4 from the present invention below (area 210).

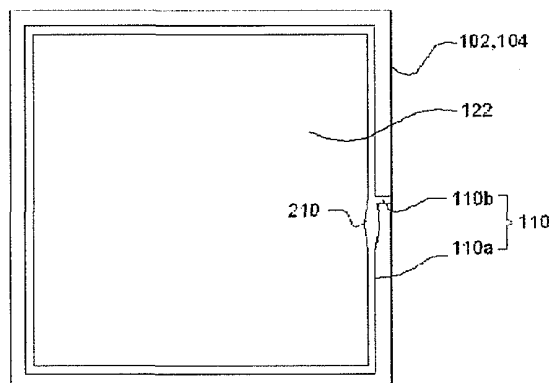


FIG. 4

Applicants submit that if anything, the *Yoshizoe* reference actually teaches away from the feature in claim 1 reciting, “the overlapping area extends along one side of the display region.” The *Yoshizoe* reference states the following:

... the sealant is coated such that the sealant is formed traveling apart gradually from the display region toward start and termination points of the sealant while overlapping a part thereof **outside** the closed loop portion and therefore, even when the two substrates are adhered to each other to

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resultantly widen the width of the sealant, the sealant never intrudes into the display region.

(Col. 2, lines 33-40; *Emphasis added.*) That is, the *Yoshizoe* reference teaches that the “overlapping area” lies outside the display region rather than extending along one side of the display region as taught in claim 1.

Accordingly, Applicants respectfully submit that independent claim 1 patently defines over *Yoshizoe* for at least the reason that *Yoshizoe* fails to disclose, teach or suggest the highlighted features in claim 1 above.

Independent Claim 5 is Patentable Over Yoshizoe

The Office Action applies the same arguments from claim 1 to reject claim 5. Claim 5 also recites the feature emphasized in claim 1 above (“wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region”). Accordingly, as discussed in the preceding section, Applicants respectfully submit that independent claim 5 patently defines over *Yoshizoe* for at least the reason that *Yoshizoe* fails to disclose, teach or suggest certain features in claim 5.

Independent Claim 11 is Patentable Over Yoshizoe

The Office Action applies the same arguments from claim 1 to reject claim 11. Claim 11 (as amended) also recites the feature emphasized in claim 1 above (“wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region”). Accordingly, as discussed in the preceding section for claim 1, Applicants respectfully

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submit that independent claim 11 patentably defines over *Yoshizoe* for at least the reason that *Yoshizoe* fails to disclose, teach or suggest certain features in claim 11.

Dependent Claims 12-13 are Patentable Over Yoshizoe

Applicant respectfully submits that dependent claims 11-13 are believed to be allowable for at least the reason that they depend from allowable independent claims. See, e.g., *In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

III. Response to Claim Rejections Under 35 U.S.C. § 103

Claims 2-4, 6, 7, and 14 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Yoshizoe* in view of Applicants' own admission. Finally, claims 8-10 and 15-18 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Yoshizoe*, in view of Applicants' own admission, further in view of *Suzuki*. For at least the reasons set forth below, Applicants traverse these rejections.

Independent Claim 8 is Patentable Over Yoshizoe, in View of Applicants' Own Admission, Further in View of Suzuki

Applicants respectfully submit that independent claim 8 patentably defines over *Yoshizoe*, in view of Applicants' own admission, further in view of *Suzuki* for at least the reason that the combination fails to disclose, teach or suggest certain features in claim 8. Claim 8 recites the same feature recited in claims 1, 5, and 11 above: "wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region." As discussed in depth and as illustrated by the figures from the *Yoshizoe* reference, the

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Yoshizoe reference does not teach this feature. Indeed, neither the *Suzuki* reference nor Applicants' own admission teach this feature either.

Accordingly, Applicants respectfully submit that independent claim 8 patently defines over *Yoshizoe*, in view of Applicants' own admission, further in view of *Suzuki* for at least the reason that the combination fails to disclose, teach or suggest the highlighted features in claim 8 above.

Independent Claim 15 is Patentable Over Yoshizoe, in View of Applicants' Own Admission, Further in View of Suzuki

The Office Action applies the same arguments used in rejecting claim 8 to reject claim 15. Applicants respectfully submit that independent claim 15 (as amended) patently defines over *Yoshizoe*, in view of Applicants' own admission, further in view of *Suzuki* for at least the reason that the combination fails to disclose, teach or suggest certain features in claim 15. Claim 15 recites the same feature recited in claims 1, 5, and 11 above: "wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region." As discussed in depth and as illustrated by the figures from the *Yoshizoe* reference, the *Yoshizoe* reference does not teach this feature. Indeed, neither the *Suzuki* reference nor Applicants' own admission teach this feature either.

Accordingly, Applicants respectfully submit that independent claim 15 patently defines over *Yoshizoe*, in view of Applicants' own admission, further in view of *Suzuki* for at least the reason that the combination fails to disclose, teach or suggest the highlighted features in claim 15 above.

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Dependent Claims 2-4, 6, 7, 9, 10 and 16-19 are Patentable

Applicant respectfully submits that dependent claims 2-4, 6, 7, 9, 10 and 16-19 are believed to be allowable for at least the reason that they depend from allowable independent claims. See, e.g., *In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

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CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

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Electronic Acknowledgement Receipt

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|---|---|
| EFS ID: | 1555293 |
| Application Number: | 10921508 |
| International Application Number: | |
| Confirmation Number: | 9818 |
| Title of Invention: | Liquid crystal display cell and method for manufacturing the same |
| First Named Inventor/Applicant Name: | Hsin-Yi Hsu |
| Customer Number: | 24504 |
| Filer: | Daniel R. McClure |
| Filer Authorized By: | |
| Attorney Docket Number: | 250330-1010 |
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| Application Type: | Utility |

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File Listing:

| Document Number | Document Description | File Name | File Size(Bytes) | Multi Part /.zip | Pages (if appl.) |
|-----------------|---------------------------------------|--------------|------------------|------------------|------------------|
| 1 | Amendment - After Non-Final Rejection | 00490757.pdf | 164323 | no | 18 |

Warnings: